

## Determining a Transistor's Maximum RF Output Power Rating

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There is a fairly wide variation between manufacturers in the method used to specify a device's rf output power. There are many factors to be considered and the foregoing explains the cause of those differences and provides a guide to a successful design.

There are several basic principles involved plus a few intangibles to make it less precise. We define drain (or collector) efficiency as

$$\eta = \frac{P_o}{P_{in}} \quad (1)$$

and then define

$$P_{in} = P_o + P_d \quad (2)$$

We can then define rf output power ( $P_o$ ) in terms of efficiency and power dissipation:

$$P_o = P_d \frac{\eta}{1-\eta} \quad (3)$$

In cases where the rf gain of the device is low and the drive power is a significant portion of the input power, i.e.  $G < 10$  dB,  $P_{in}$  should include the drive power. In this case it is called power-added efficiency, PAE.

The rest of the exercise, the more difficult part, involves determining a reasonable value for  $P_d$ . This is not the value given on the data sheet. That one is based on the theoretical and unrealizable conditions of holding the junction at  $T_j(\text{max})$  and the case at 25°C. Regardless of the output power specification, every manufacturer's data sheet provides a value for the junction-to-case thermal resistance,  $R\theta_{jc}$ . This is determined by several methods including infrared measurement and then is derated to a maximum value to cover the range of typical manufacturing variations. This quantity must then be added to the other thermal interface resistances to determine

the total thermal impedance from the semiconductor junction out to thermal ambient.

A power transistor is typically mounted on a heat sink with thermal grease to reduce the effects of gaps in the mechanical interface between its mounting surface and the heat sink. Every effort should be made to insure that both mating surfaces are as flat and smooth. The greased interface will typically add about  $0.1 \text{ }^\circ\text{Cin}^2/\text{W}$ . That means a device with 0.5 sq in of package base area will have a case-to-sink thermal impedance ( $R\theta_{cs}$ ) of  $0.2 \text{ }^\circ\text{C/W}$ , half the area, twice the resistance.

The heat sink has a thermal impedance too and it is generally the largest design variable in the system. Depending on the construction and method of cooling, the heat sink's thermal resistance,  $R\theta_{sa}$ , from sink-to-ambient can range from  $0.1^\circ\text{C/W}$  for a water-cooled copper block to  $25^\circ\text{C/W}$  or more for a clip-on sink in still air. Regardless of the heat exchange medium transferring the heat from the sink to the ambient environment, it is important to consider the maximum temperature specified. If the air-cooled sink will operate inside a car in the sun,  $50^\circ\text{C}$  should be the ambient design temperature.

Thermal impedances add in series so for a total system the thermal resistance between the transistor junction and the ambient is the sum of all the interface impedances:

$$R\theta_{ja} = R\theta_{jc} + R\theta_{cs} + R\theta_{sa} \quad (4)$$

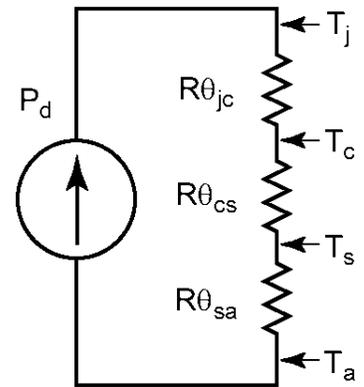
All manufacturers specify a maximum operating junction temperature for their devices,  $T_j(\text{max})$ . This is typically  $200^\circ\text{C}$  for air-cavity ceramic-metal packaged parts and  $150^\circ\text{C}$  for plastic-encapsulated parts. This is the maximum transistor junction temperature before irreparable damage is done. However, it has been shown in many

studies that high operating temperatures are very detrimental to the operational life and reliability of semiconductor devices. Most companies have design guidelines that define the maximum and typical operating junction temperatures for semiconductor parts within a system.  $130^\circ\text{C}$  is a good value for a typical design.

Power and thermal resistance are related in a similar way to Ohm's Law where current is replaced by power dissipation and voltage drop is replaced by temperature differential.

$$\Delta T_{ab} = R\theta_{ab} \times P_d \quad (5)$$

For a given amount of power dissipated by a device, each thermal impedance develops a temperature drop across itself. The higher the thermal resistances, the higher the junction temperature rises above a given ambient.



The transistor manufacturer sets the absolute limit on maximum junction temperature, which is then lowered by the designer to meet system reliability goals. The maximum ambient temperature is set by the system specifications. The designer must then provide the minimum heat sink impedance to satisfy these conditions.

As an example, assume we are designing an amplifier using a device with  $R\theta_{jc}$  of  $0.5^\circ\text{C/W}$ . Though it is rated for use to up to a  $T_j(\text{max})$  of  $150^\circ\text{C}$ , we will use  $130^\circ\text{C}$  as the maximum allowed to improve reliability and provide some "distress margin". The amplifier will be mounted on a large air-cooled heat sink with an  $R\theta_{sa}$  rating of  $.8^\circ\text{C/W}$ . The part will be mounted on the

sink using high quality thermal grease that gives a mounting resistance of 0.2°C/W. Thus the total resistance,  $R\theta_{ja}$ , is 1.5°C/W. If the maximum ambient within the system's operating environment is 50°C, we have enough information to calculate the available device dissipation. From equation (5) we calculate

$$P_d = \frac{\Delta T}{R\theta_{ja}} = \frac{130 - 50}{1.5} = 53.3 \text{ Watts.}$$

Now we can return to the original question – how much output power? That depends on the type of amplifier, its class of operation and efficiency. For a typical class C amplifier, 75% is a reasonable static efficiency when operated into a matched load. If the output is a 100% CW carrier, equation (3) gives

$$P_o = 53.3 \times \frac{.75}{1-.75} = 160 \text{ Watts.}$$

This assumes a flat load. If any additional dissipation is required to meet the ruggedness requirements of a non-matched load, typically resulting in a lower operating efficiency, that must be factored in as well.

If the waveform is not CW higher peak power is possible provided the pulse width is less than the thermal time constant of the junction and package and the average power calculated for CW is not exceeded. Most data sheets show a relationship between pulse width, duty cycle and effective  $R\theta_{jc}$ , the transient thermal impedance.

At this point it should be easier to understand the manufacturers' difficulty specifying an output power. There are many variables that must be set to get to a final answer. Most manufacturers use the performance numbers provided in their standard test circuit. The class of operation

and duty cycle are specified as well as a minimum efficiency into a matched load, and sometimes a ruggedness rating (pass/fail) at some higher load VSWR, but nothing is ever said about mounting or cooling.

Therefore when comparing the output power capability of several devices the most important number on the specification sheet is  $R\theta_{jc}$ . This number is fixed by the device construction and means the same thing for all devices regardless of the manufacturer. All of the other operating conditions that determine the device's maximum output power are defined by the user's application.

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