Frequencies generated by the BFO board and PTO modules are routed to the IF board mixing stages where they are utilized by both transmit and receive circuitry. An explanation of signal processing in these circuits and other circuits that are common to both transmit and receive modes is covered in paragraph 3.4.

The theory of operation section employs the use of simplified diagrams to supplement the text. Complete schematics are contained in Section VI and should be used in conjunction with the simplified diagrams to determine electrical values and relationships.

3.2 TRANSMITTER CIRCUITRY

3.2.1 Transmit Signal Path

A stage-by-stage transmit signal path block diagram is shown in Figure 3-2. Unless otherwise indicated in the following explanation, it is assumed that the CX7 is operating in the single sideband mode.

Audio signals from the microphone connector J2, on the Model CX7 front panel, are routed to pin 301 on the Audio board, and then to the base of transistor Q1. The nominal signal level at this point is 10 millivolts rms, for frequencies in the range of 400 to 3000 Hz. The audio signal is amplified by transistor Q1 and then routed through variable resistor R12 and coupled to the base of Q2. Phone patch signals from J11, on the rear panel of the CX7, are also routed to the base of transistor Q2 via pin 325 on the Audio board. The amplified output of transistor Q2 is routed through transistor Q3, which is operating as an emitter follower, to output pin 330 on the Audio board. The nominal value of the signal at the output of the Audio board is 100 millivolts, peak-to-peak.

The signal from the Audio board is applied to the AGC Detector input pin 501 and is then routed to one input of the balanced modulator. The balanced modulator is comprised of balanced transformers T1 and T2 and hot carrier diodes CR4 through CR7. The second input of the balanced modulator is a 8.8 MHz carrier signal having a nominal level of 1 VRMS. The 8.8 MHz carrier signal originates in the BFO board and is directed to the balanced modulator via pin 212, on the BFO board, and pin 495 on the AGC Detector board. The balanced modulator mixes the 8.8 MHz carrier with the audio signal to produce a resultant 8.8 MHz double sideband signal with the carrier suppressed approximately 40 DB. The third and higher order modulation products are also suppressed approximately 40 DB below each sideband. The balanced modulator output is routed to the AGC Detector board output pin 500 where the nominal RK signal level is 2 volts peak-to-peak.

The RF signal from the output of the AGC Detector board is applied to IF board input pin 435 and then to one input gate of the dual gate field effect transistor Q14. The other input gate of transistor Q14 is utilized for establishing the clipping level in this stage. The double sideband 8.8 MHz signal is amplified by transistor Q14 and is routed through the 25 kHz bandpass filter FL3 to field effect transistor Q11. The amplified output of transistor Q11 is routed through the 2.4 kHz bandpass filter FL1 to integrated circuit IC5 and IC3. The function of the IC5 stage is to provide further amplification to drive transistor Q5 which is operating as a clipping indication meter amplifier. The function of the IC3 stage is to amplify the double sideband 8.8 MHz signal and to operate as an RF clipper. RF levels at the output of the IC3 stage exceeding 450 millivolts rms, are clipped and routed through an additional 2.4 kHz bandpass filter FL2 to gate G1 of dual gate field effect transistor Q8. When the CX7 is operating in the AM or CW mode, dual gate field effect transistor Q8, on the AGC Detector board, is switched on to provide an 8.8 MHz carrier that is also applied to gate G1 of transistor Q8 on the IF board. (The 8.8 MHz carrier is modulated by one of the sidebands at gate G1 of transistor Q8 on the IF board when in the AM mode.) The other input gate of transistor Q8 is receiving a frequency derived from the mixer stages that are discussed in paragraph 3.4.4. Transistor Q8 on the IF board operates as a mixer and combines the signals on both gates to provide a 39 to 40 MHz IF output that is applied to IF board output pin 421. The RF signal level at pin 421 is a nominal value of 50 millivolts peak-to-peak, and it is routed to the Front End board.

The 39 to 40 MHz RF signal from the IF board is connected to the Front End board input pin 68 and then to field effect transistor Q4. This stage operates as a low noise RF amplifier and its output is applied to integrated circuit IC1. A frequency, determined by the setting of the MHZ bandswitch S7 located on the front panel of the CX7, is generated by crystal oscillator transistor Q7 and is also applied to integrated circuit IC1. The function of IC1 is to mix the 39 to 40 MHz RF signal and the crystal oscillator output to produce a resultant difference frequency. The output of integrated circuit IC1 is routed through a low pass filter comprised of inductors L3 and L4 and capacitors C40 through C43 to the base of transistor Q5 operating as an emitter follower. The output of transistor Q5 is applied to the Front End board output pin 59. The RF

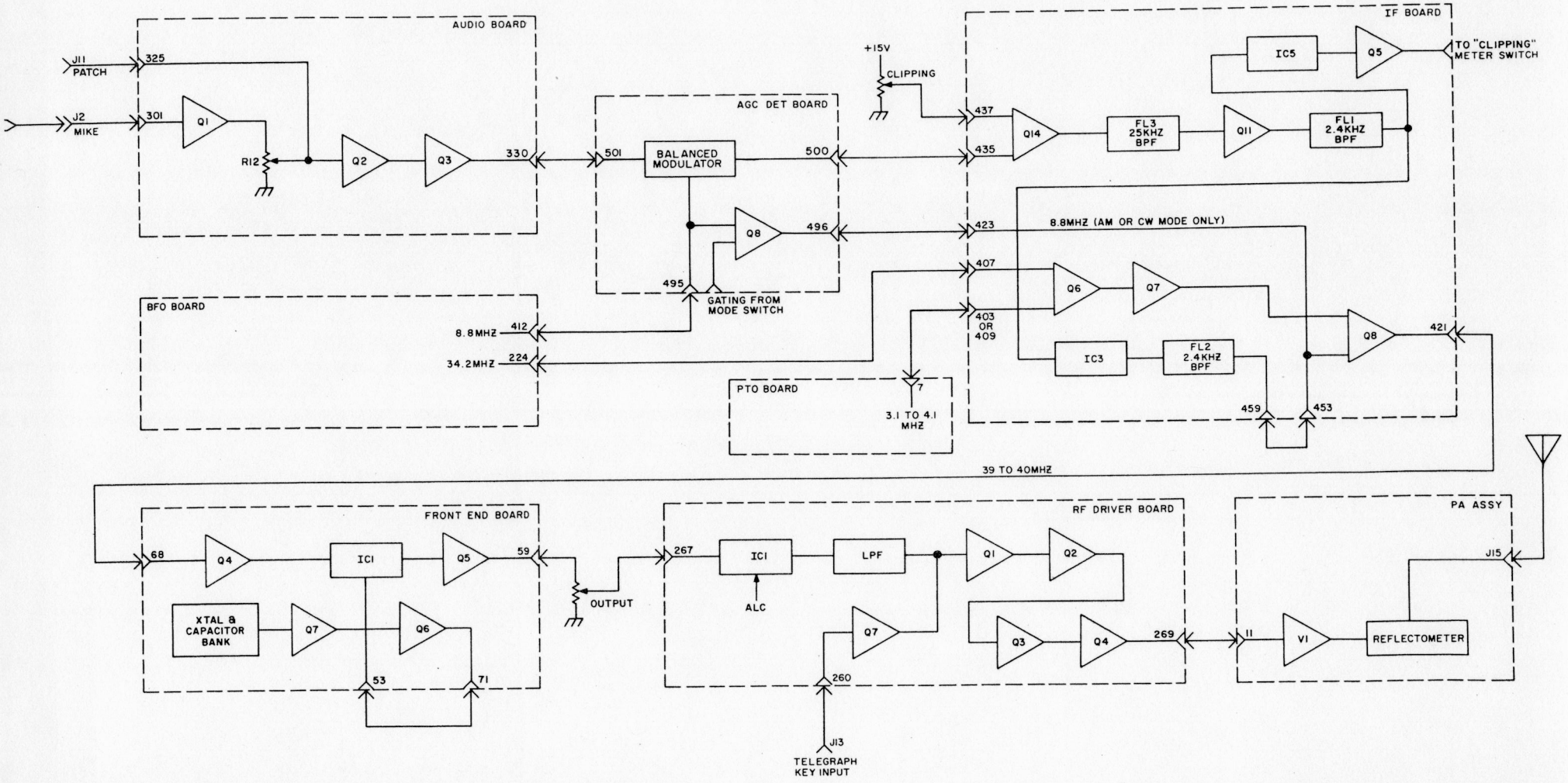


Figure 3-2. Transmit Signal Path Block Diagram

signal level at pin 59 is a nominal value of 300 millivolts, peak-to-peak, and is routed to "OUTPUT" potentiometer R9, located on the front panel of the CX7.

The desired transmit frequency is routed from the wiper of potentiometer R9 to the RF Driver board input pin 267 and then to integrated circuit IC1. This stage operates as a linear differential amplifier receiving automatic level control (ALC) bias to govern the output of the RF drive. The output of integrated circuit IC1 is directed to a low pass filter comprised of inductors L1 and L2 and capacitors C8 through C11. The low pass filter output is directly applied to the gate of field effect transistor Q1. When in the CW mode, the operation of transistor Q1 is enabled or inhibited by the waveshaping amplifier transistor Q7 being turned on or off by command signals from the hand or paddle telegraph key. The amplified output of transistor Q1 is routed through an RF amplifier chain comprised of transistors Q2 through Q4. The operating frequency range of integrated circuit IC1 and transistors Q2 through Q4 is from 1.8 to 30 MHz. Wide band operation without gang tuning is accomplished in these stages by utilizing broad band toroidal coupling transformers and standard degenerative video amplifier techniques. The output of the RF amplifier transistor Q4 is applied to the RF Driver board output pin 269. The RF signal level at this point is approximately 40 volts, peak-to-peak.

The RF output of the RF Driver board is routed to the PA Assembly input pin 11 and is then applied to the control grid of power amplifier tube V1. The power amplifier tube is operating in a grounded cathode passive grid configuration. The output of tube V1 is routed through a toroidal Pi-L network, utilized for plate tuning, to the Reflectometer Assembly. The reflectometer circuitry operates as a power sensor that derives output voltages from the RF current flowing through it. The derived voltages are representative of the forward and reverse power and are utilized for metering purposes. After the RF output of tube V1 passes through the plate tuning circuits and Reflectometer Assembly, it is applied to the main antenna connector J15, located on the CX7 rear panel. The RF power output at connector J15 is a nominal 150 watts on all bands.

3.2.2 Automatic Level Control

Automatic Level Control (ALC) is employed to control the amount of RF drive to the power amplifier tube V1. The ALC method utilized by the CX7 is shown in simplified diagram Figure 3-3. The conduction of transistor Q5 on the RF Driver board is the center of RF drive control and also establishes the fixed operating bias of -20 VDC on the control grid of tube V1. When the base of transistor Q5 is reverse biased by the absence of a ground, the fixed control grid bias drops to -60 VDC thereby cutting-off the plate current. The ground that is used to forward bias the base of transistor Q5 originates in the PA Assembly chassis. It is routed through the energized relay K1 contacts 5 and 12, the PA Assembly output pin 5, the energized one minute time delay relay K1 contacts 4 and 9 (located on the CX7 chassis), the rear panel connector J5 pins 3 and 2, the RF Driver board input pin 259 to one end of variable resistor R31. With no RF drive and the ground present, variable resistors R31 and R34 are adjusted to limit the idling plate current of tube V1 to 100 MA and a transistor Q5 collector potential of zero vdc.

Integrated circuit IC1 functions as a differential amplifier passing maximum RF drive when no ALC voltage is present. The increased conduction of transistor Q5 provides the ALC voltage whenever grid current is drawn by tube V1. The increased collector current of transistor Q5 causes the collector potential to go negative. When the collector voltage of transistor Q5 reaches -12 VDC, zener diode CR1 conducts and the ALC voltage is then applied to integrated circuit IC1 resulting in an inversely proportional decrease in RF drive. The -12 VDC hold-off permits tube V1 to draw its normal 3 MA of grid current due to premature grid emission.

An ALC voltage is also generated by the screen grid current of tube V1. When the voltage drop across Power Supply board resistor R6 exceeds -3.9 vdc, zener diode CR2 conducts and provides a control voltage to integrated circuit IC1.

RF Driver board transistor Q6 functions as a meter amplifier. It amplifies either or both of the ALC voltages.

3.2.3 Sidetone

When the CX7 is in the CW mode, the sidetone circuitry provides an audio tone permitting the code transmission to the RF circuits to be monitored.

A simplified diagram of the sidetone circuitry is shown in Figure 3-4. The audio frequency is generated by the phase shift oscillator transistor Q5, located on the Audio board. In the AM, LSB, and USB modes, the operation of transistor Q5 is inhibited by the presence of a ground being applied to Audio board input pin 319. There are two paths utilized in connecting a ground to pin 319. The first path is through the "MODE" switch S8D contacts 6 and 7, 8, or 9, to ground at E8. The second path is through the "MODE" switch S8D contacts 6 and 10, 11, or 12, and the energized "TUNE" switch S1D contacts 8 and 9 to ground at TB1-6.

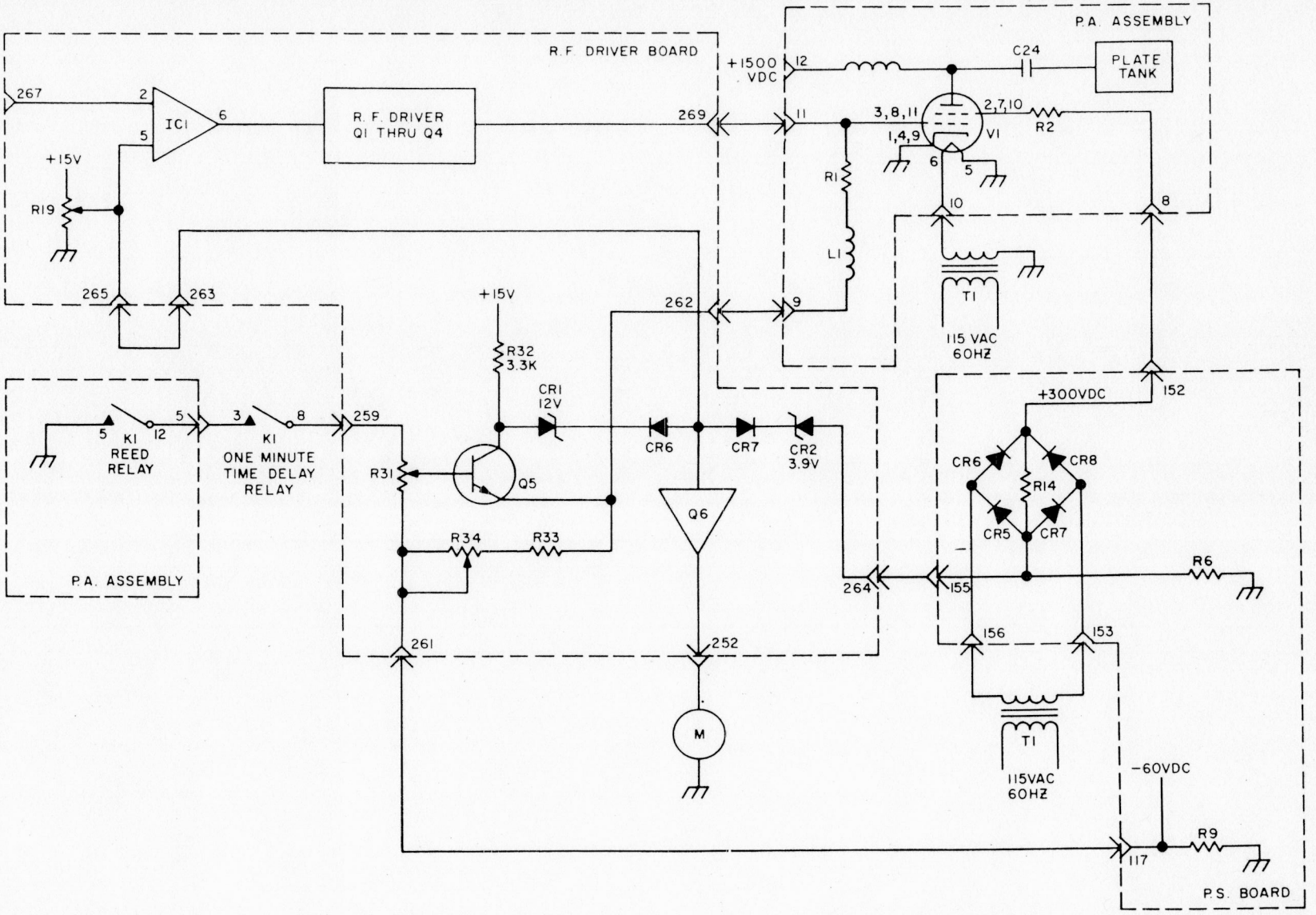


Figure 3-3. Automatic Level Control Simplified Schematic Diagram

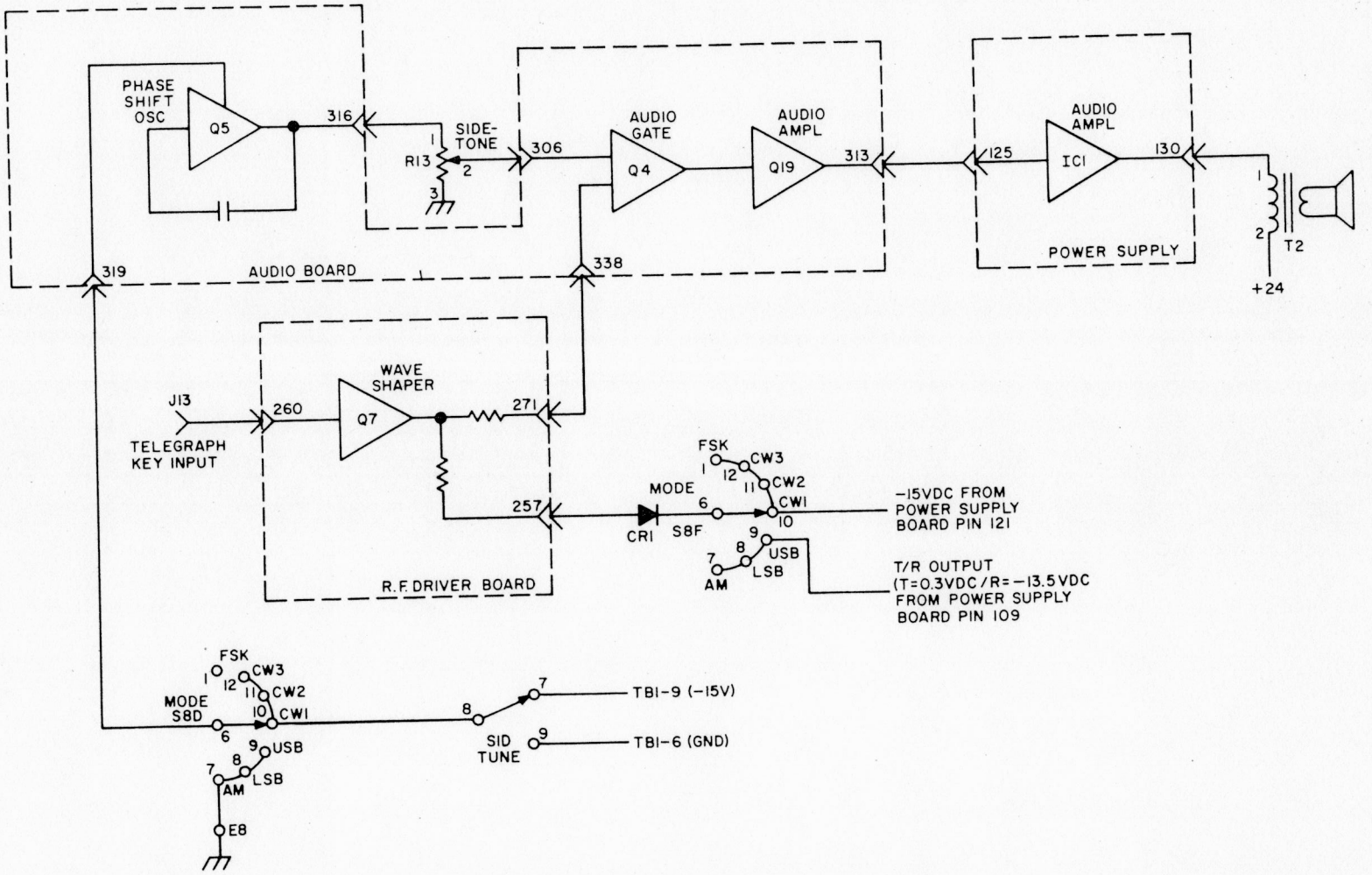


Figure 3-4. Sidetone Simplified Schematic Diagram

In any CW mode and when the "TUNE" switch S1D is in the deenergized position, the operation of transistor Q5 is enabled by the presence of -15 VDC. This is accomplished by routing -15 VDC from TB1-9 through the "TUNE" switch S1D contacts 7 and 8 and the "MODE" switch S8D contacts 10, 11, or 12 and 6 to Audio board pin 319. The audio output signal of the oscillator is connected to Audio board output pin 316 and is then routed to the "SIDETONE" potentiometer R13, located on the CX7 rear panel. The audio tone from the wiper of potentiometer R13 is connected to Audio board input pin 306 and coupled to the source of field effect transistor Q4 which is utilized to gate the audio signal. Transistor Q4 is normally being inhibited by a negative potential routed from the Power Supply board via "MODE" switch wafer S8F contacts 10, 11, or 12 and 6, RF Driver board input pin 257, output pin 271, and Audio board input pin 338. Waveshaping transistor Q7 on the RF Driver board also is normally in an off condition. When an energized telegraph key routes a ground via connector J3 pin 1 on the CX7 rear panel and RF Driver board input pin 260 to the base of transistor Q7, the negative potential inhibiting transistor Q4 is removed by transistor Q7 switching to an "on" condition. This can also be caused by the Counter board keyer output applying a ground to RF Driver board pin 260. The audio signal is then permitted to pass through audio gate transistor Q4 and is amplified by field effect transistor Q19. The audio output of transistor Q19 is connected to Audio board output pin 313 and is routed to Power Supply board input pin 126 and then applied to integrated circuit IC1 which is functioning as a linear audio amplifier. The audio output of integrated circuit IC1 is routed to Power Supply board output pin 130 and then to the primary of audio output transformer T2 located on the CX7 inside rear panel. The secondary of transformer T2 is connected to the "PHONES" connector J1 on the CX7 front panel and to the "SPKR" connector J3 on the CX7 rear panel. Connectors J1 and J3 are interwired so that the speaker output is interrupted whenever the headphones are connected. Transformer T2 also provides a 600-ohm output to "POWER" connector J6 pins 4 and 5.

During voice modes, the operation of the Audio Gate transistor Q4 is enabled by the presence of the +0.3 volt potential in the T/R code but the operation of the phase shift oscillator is inhibited.

3.2.4 Transmitter Enabling

Transmitter enabling is defined as satisfying the pre-requisit conditions that must be present before either RF drive or output power can be developed by the transmitter circuitry.

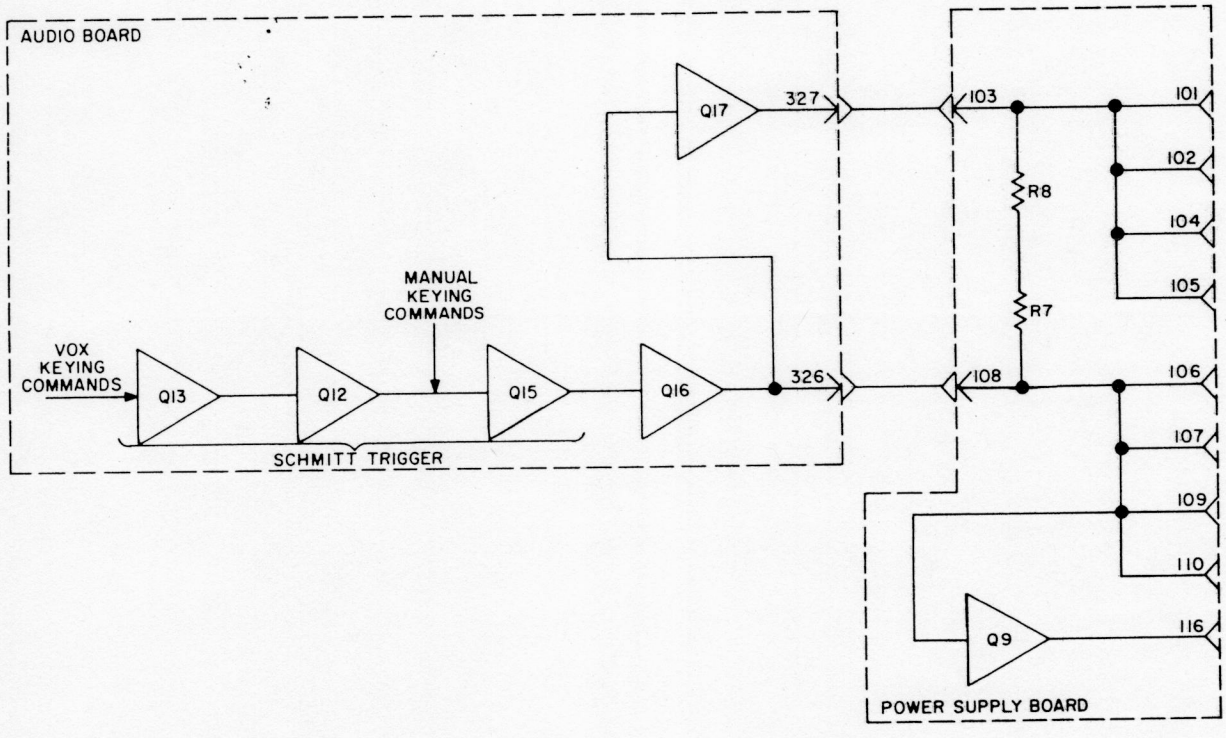


Figure 3-5. T/R and R/T Command Simplified Schematic Diagram

T/R and R/T Commands

Transmit/Receive (T/R) and Receive/Transmit (R/T) commands are complementary voltages, utilized to enable the operation of the transmitter circuits and inhibit the operation of the receiver circuits.

T/R Command

The potential of the T/R command is +0.3 VDC in the transmit mode and -13.5 VDC in the receive mode. Model CX7 wiring utilizes green insulation for the T/R lines. A simplified diagram depicting how the T/R commands are generated is shown in Figure 3-5. The master control for the T/R command is the Schmitt Trigger circuit located on the Audio board. Switching the output state of the Schmitt Trigger can be accomplished either manually or automatically. The desired state of the Schmitt Trigger for a transmit condition is to switch transistor Q15 to an "OFF" condition. This permits the negative collector potential of transistor Q15 to reverse bias the base of transistor Q16 thereby maintaining the collector potential of transistor Q16 at +0.3 volt. This potential is routed to Audio board output pin 326 and then to Power Supply board input pin 108, which is used as a distribution point for the T/R command. The +0.3-volt potential is distributed throughout the CX7 as shown in diagram Figure 3-6.

A -13.5 VDC potential is also used to enable portions of the transmitter circuitry. The base of Power Supply board transistor Q9 is forward biased by the +0.3-volt potential. When this occurs, transistor Q9 provides a -11.1 VDC output that is routed to Power Supply board output pin 116, PA Assembly input pin 2 and then to the coil of reed relay K1 pin 1 which together with the +34 VDC on the other side of the coil causes the relay to energize. When energized, relay K1 grounds the front end of the receiver circuitry and provides a ground to enable the operation of the ALC circuitry.

R/T Command

The potential of the R/T command is +0.3 VDC in the receive mode and -13.5 VDC in the transmit mode. Model CX7 wiring utilizes grey insulation for the R/T lines. The R/T command is generated as shown in Figure 3-5. The +0.3-volt

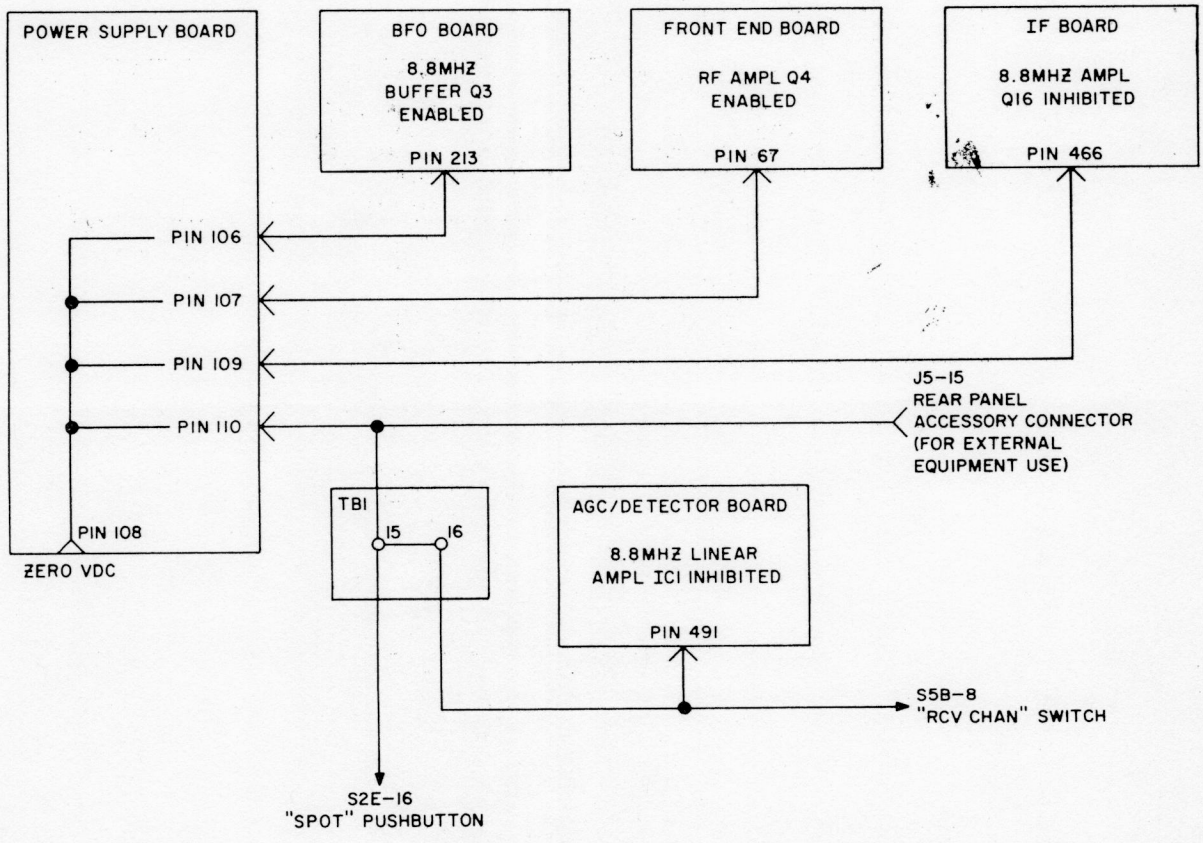


Figure 3-6. T/R Distribution Block Diagram (Transmit Mode)

potential of the T/R command is utilized to forward bias the base of Audio board transistor Q17. This in turn causes transistor Q17 to provide a -13.5 VDC output that is routed to Audio board output pin 327 and Power Supply board input pin 103. Pin 103 is used as a distribution point for the -13.5 VDC potential of the R/T command as shown in Figure 3-7.

Vox Keying

When operating in a voice mode, transmitter enabling is accomplished automatically by the "VOX" circuitry. A VOX keying block diagram is shown in Figure 3-8. Audio signals from the microphone are routed to CX7 front panel "MIKE" connector J2 pin 1 and then to Audio board input pin 301 where it is coupled to the gate of field effect transistor Q1. The amplified audio signal from the output of transistor Q1 is routed to Audio board output pin 336 and then applied to one end of the rear panel "VOX GAIN" variable resistor R10 on the CX7 rear panel. The audio signal from the wiper of variable resistor R10 is routed through the energized front panel "VOX" switch S1E contacts 3 and 2 to Audio board input pin 322 where it is coupled to the base of transistor Q6. The audio signal is amplified by transistor Q6 and is coupled to the base of transistor Q7 for additional amplification. The output of transistor Q7 is coupled to the base of transistor Q8. The base of transistor Q8 is solely dependent on the amplified audio signal for forward bias. When transistor Q8 is forward biased it provides a negative potential that in turn forward biases transistor Q12 causing it to switch to an "ON" condition. The function of the forward biased transistor Q12 is to provide a negative potential to forward bias transistor Q13 in the Schmitt Trigger circuit. When transistor Q12 is switched to an "ON" condition, it also causes the Darlington connected transistors, Q13 and Q14, shown in Figure 3-5, to switch to an "ON" condition which in turn drives transistor Q15 to an "OFF" condition. The "OFF" condition of transistor Q15 is the required output state of the Schmitt Trigger circuit (a negative potential at the collector of Q15). The rear panel "DELAY" potentiometer R12 is used to vary the RC time constant in the emitter of Q12 on the Audio board. With the switching transistor Q12 forward biased by a "VOX" signal, capacitor C28 charges to approximately -14 VDC. Whenever the voltage at the emitter of transistor Q12 drops below the threshold voltage of the Schmitt Trigger, the Schmitt Trigger rapidly switches to its normal state; thereby providing a very positive change of states at its output. This may cause the transmitter to unkey between

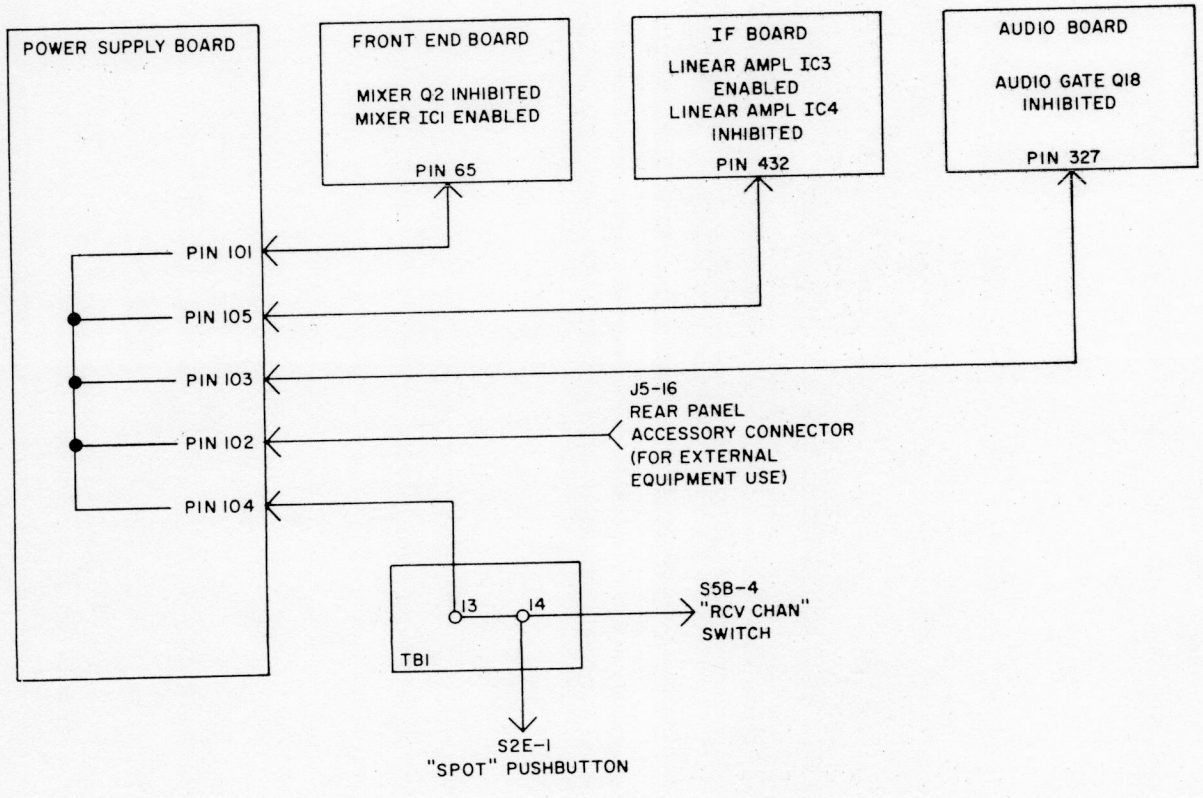


Figure 3-7. R/T Distribution Block Diagram (Transmit Mode)

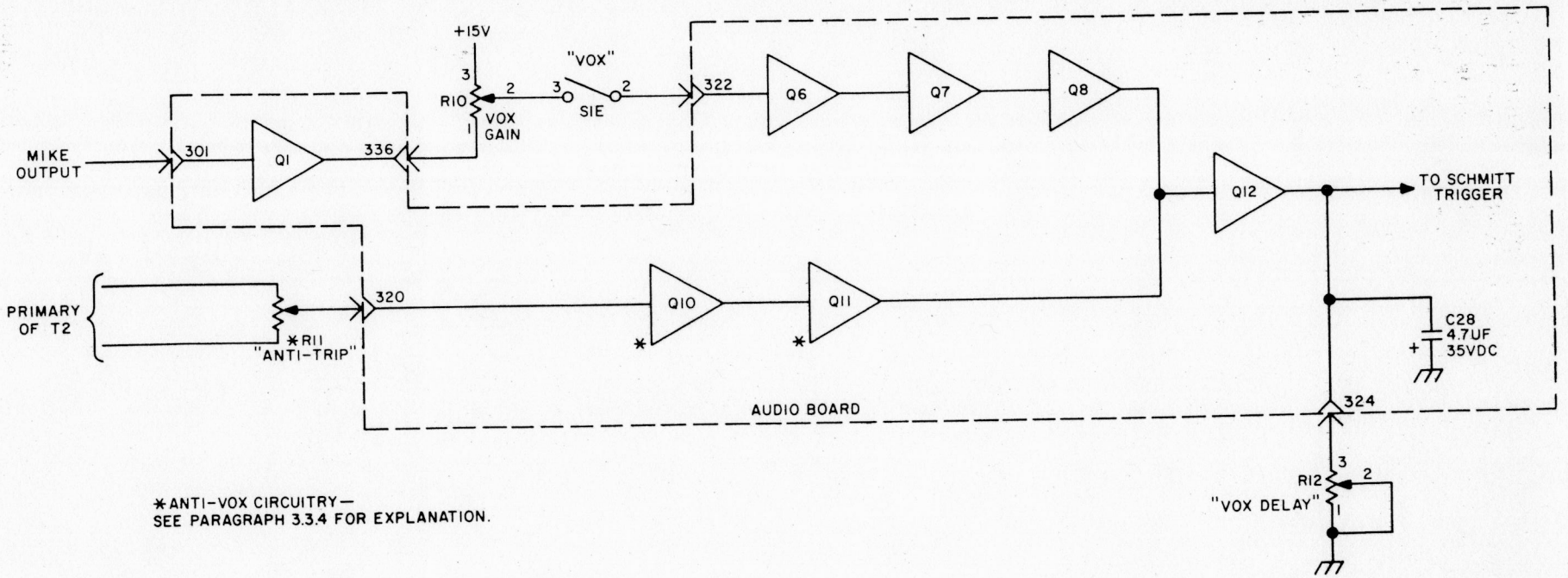


Figure 3-8. VOX Keying Simplified Schematic Diagram

spoken syllables of a lower speech rate. Therefore, it is desirable to keep the transmitter keyed a few milliseconds longer. This is accomplished by increasing the resistance setting of the "DELAY" potentiometer R12 thereby increasing the discharge time of capacitor C28, which in turn, momentarily retains the required base bias of the Schmitt Trigger transistor Q13.

Manual Keying

If it is not desired to use the "VOX" method while operating in the voice mode, transistor Q15 can be switched to an "OFF" condition by either manually depressing the front panel "CONTROL-XMIT" switch S1C or the "CONTROL-TUNE" switch S1D or by energizing an external push-to-talk switch on the microphone. A Manual Keying Signal Path diagram is shown in Figure 3-9.

When either of the previous operations are performed, the forward base bias of Schmitt Trigger transistor Q15 is shorted to ground via Audio board input pin 329, RF Driver board output pin 258, diode CR5, and RF Driver board input pin 260. The ground is provided to RF Driver board pin 260 from terminal board TB1 pin 6 through the energized "CONTROL-XMIT" switch S1C contacts 3 and 2, and "MODE" switch S8C contacts 6 and 1, 9, 7 or 8. The energized "CONTROL-TUNE" switch S1D contacts 5 and 6 can also provide a ground to pin 260. The microphone push-to-talk line from "MIKE" connector J2 pin 3 is another ground source.

When operating in the "FSK" or any "CW" mode, Schmitt Trigger transistor Q15 is switched to an "OFF" condition in a similar manner by routing a ground from the Counter board keyer output

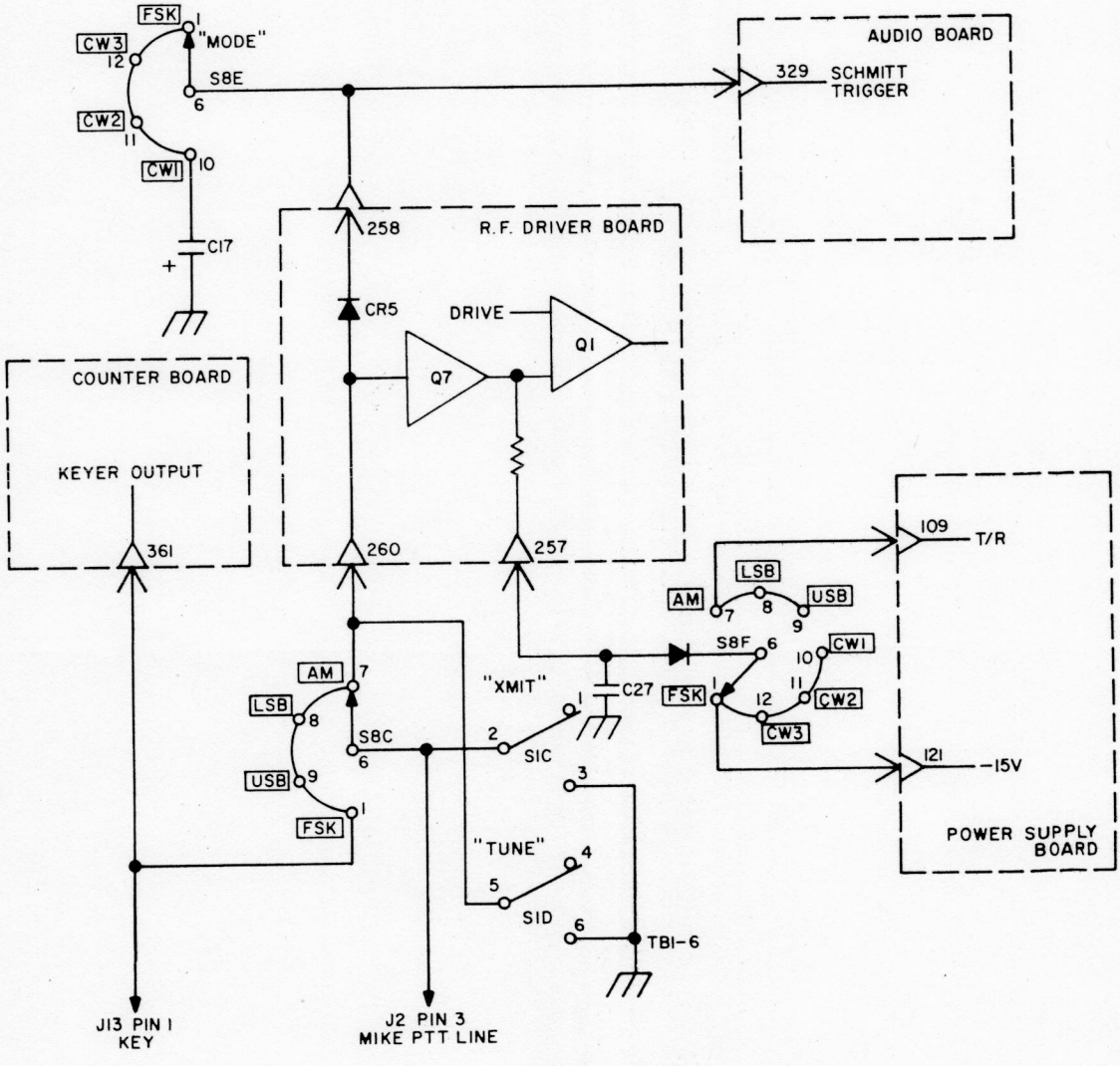


Figure 3-9. Manual Keying Simplified Schematic Diagram

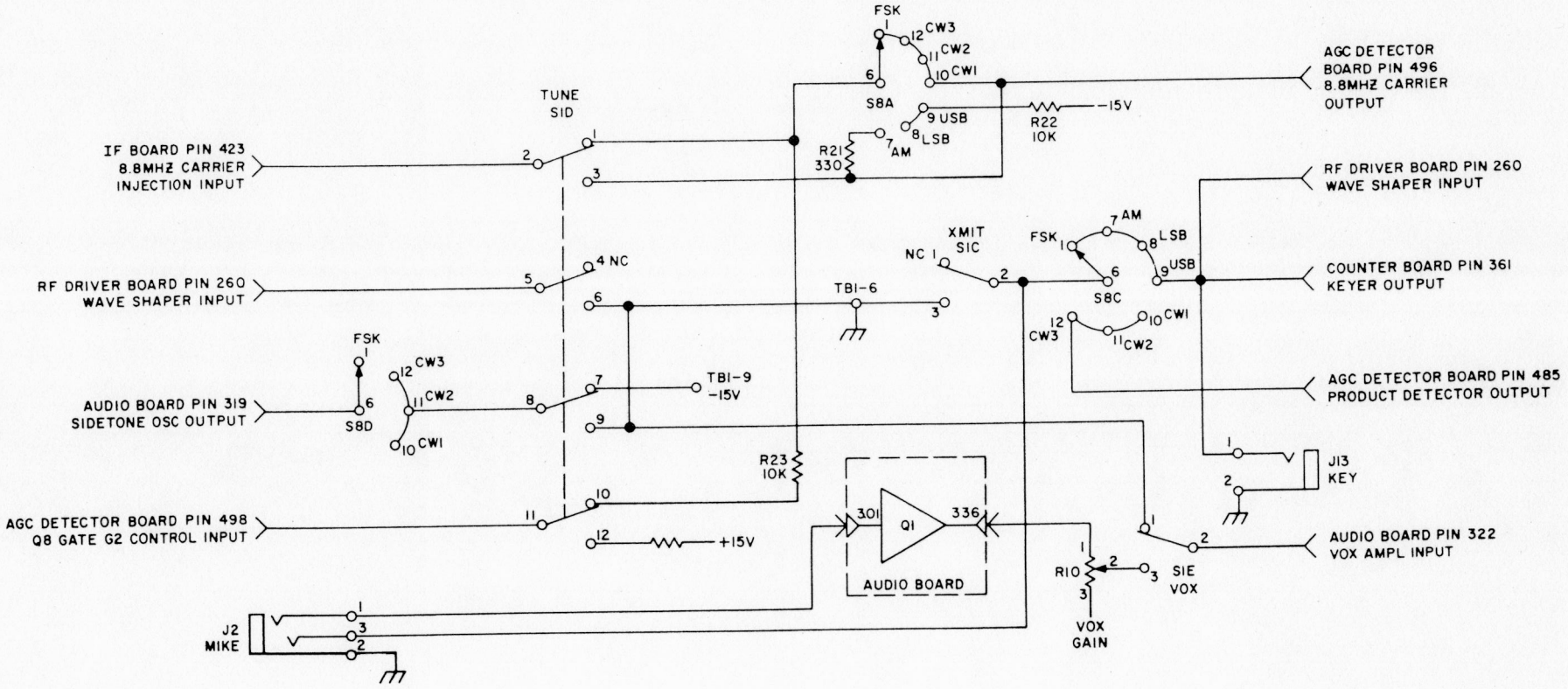


Figure 3-10. Transmit Control Switching Simplified Schematic Diagram

pin 361 or from the rear panel "EXT KEY" connector J13 pin 1 to Audio board input pin 329. In these modes, the ground must also be used to enable the operation of the RF driver circuit. This is accomplished by utilizing the ground to forward bias the base of transistor Q7, which in turn, removes the negative potential that is inhibiting the gate of field effect transistor Q1. With the negative potential removed, transistor Q1 is permitted to amplify the RF drive. The function of transistor Q7 is to increase the rise and fall time of the CW keying signal thereby improving its RF envelope waveshape. Note that the output of transistor Q7 is not used in the voice mode because the T/R command at Power Supply board output pin 109 has switched from -13.5 VDC to +0.3 VDC for a transmit condition. The purpose of capacitor C27 is to lengthen the rise time of the transmitted signal so that full RF output will not instantaneously appear while in the VOX mode. This protects the circuitry of the Model CX7 when used in conjunction with a linear amplifier.

3.2.5 Transmit Control Switching

Transmitter circuitry control switching is accomplished by the proper positioning of front panel "CONTROL-PTT, -TUNE, -XMIT or -VOX" switches. The switches are interconnected as shown in simplified diagram Figure 3-10.

In normal operation, only one of the "CONTROL" switches will be energized at a time and the others will be deenergized. The "CONTROL-PTT" switch is not electrically connected to any circuit and its only function is to mechanically deenergize the remaining "CONTROL" pushbuttons thereby placing the CX7 in the receive mode. The "CONTROL-VOX" switch S1E and the "CONTROL-XMIT" switch S1C were previously discussed in paragraph 3.2.4 for an energized condition. When the "CONTROL-VOX" switch S1E is in the deenergized position, a ground from terminal board TB1-pin 6 is connected to the signal input line of the "VOX" amplifier circuitry on the Audio board. When the "CONTROL-XMIT" switch S1C is in the deenergized position it is in an open circuit condition providing no electrical connections. "CONTROL-TUNE" switch S1D provides the following three interconnections when in the deenergized position: First, a ground is routed from terminal board TB1-pin 6 through contacts 1 and 2 to IF board input pin 423. The ground prevents any stray signals from being introduced into the system at this point when not in the "TUNE" mode. Second, a gating potential from "MODE" switch S8A is routed through resistor R23 and contacts 10 and 11 to AGC Detector board input pin 498 and then to the G2 gate of dual gate field effect transistor Q8. When "MODE" switch S8A is in the "AM", "CW1", "CW2", "CW3" or "FSK" position the gating potential is a positive voltage and in the "LSB" or "USB" position the gating potential is a negative voltage. Third, a -15 VDC potential from Terminal board TB1 pin 9 is routed through contacts 7 and 8 and the "MODE" switch contacts 10, 11, or 12 and 6 to Audio board input pin 319 where it enables the operation of the sidetone oscillator. Energizing (depressing) the "CONTROL-TUNE" switch S1D mechanically causes the "CONTROL-XMIT" switch S1C or the "CONTROL-VOX" switch S1E to deenergize. It also completes the following four electrical interconnections: First, a ground from terminal board TB1 pin 6 is routed through contacts 6 and 5 to RF Driver board input pin 260 which is the key line. Second, a ground from terminal board TB1 pin 6 is routed through switch S1D contacts 9 and 8 and "MODE" switch S8D contacts 10, 11 or 12 and 6 to Audio board input pin 319 where it inhibits the operation of the sidetone oscillator. Third, a +15 VDC potential is routed through contacts 12 and 9 to AGC/Detector board input pin 498 where it is used to forward bias the gate G2 of dual field effect transistor Q8. Under this condition, transistor Q8 passes an 8.8 MHz signal that is then applied to AGC/Detector board output pin 496. Fourth, the signal from AGC/Detector board output pin 496 is routed through switch S1D contacts 3 and 2 to IF board input pin 423 where it is injected into the transmit signal path. The CX7 transmitter circuitry is now fully enabled. This permits manual tuning or testing to be performed. A constant carrier CW output will be present when the Model CX7 is properly tuned.

3.2.6 Automatic Keyer

The automatic keyer circuitry is located on the Counter board. A block diagram of the keyer is shown in Figure 3-11. It is comprised of integrated circuits IC15 through IC17, transistors Q3, Q5, and Q8, and front panel "KEYER SPEED" potentiometer R4. The objective of the keyer is twofold. First, it must not provide an output when unkeyed. Second, when keyed, it provides an automatic dot or dash output that can be adjusted for operating speeds of 5 to 60 words per minute. Unlike the other circuitry on the Counter board, it does not use a clock frequency derived from the 100 kHz oscillator. It has its own frequency source derived from the multivibrator oscillator comprised of transistors Q3 and Q5.

The keyer circuitry will always be in one of three basic conditions as follows: First, the keyer may be in an unkeyed condition. Second, the keyer may be in a condition keyed for a dash. Third, the keyer may be in a condition keyed for a dot.

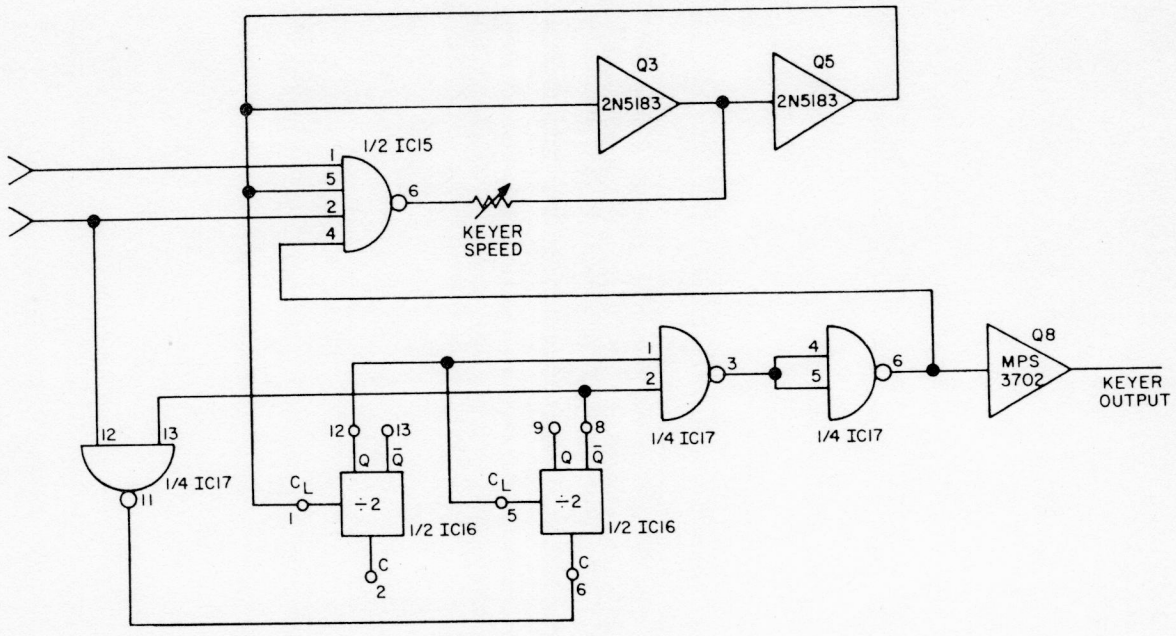


Figure 3-11. Automatic Keyer Logic Block Diagram

In an unkeyed condition, the multivibrator oscillator is not operating because the output state of integrated circuit IC15 at pin 6 is not supplying a positive potential to forward bias the base of transistor Q5. The following unkeyed conditions for the remaining circuitry was produced by the completed dot or dash cycling of events: Integrated circuit IC16 output pin 12 and 8 are at a positive potential causing the output of integrated circuit IC17 pin 3 to be driven to a ground potential which in turn drives IC17 output pin 6 to a positive potential, thereby reverse biasing the base of transistor Q8. Integrated circuit IC15 input pins 1, 2, 4, and 5 each has a positive potential being applied, thereby driving its output at pin 6 to a ground potential.

In a "DOT" condition, a ground is routed from an external speed key to rear panel "KEYER" connector J12 pin 3 then to Counter board input pin 363 and is applied to integrated circuit IC15 input pin 1. The ground causes integrated circuit IC15 output pin 6 to be driven to a positive potential thereby forward biasing the base of transistor Q5. When this happens, the collector potential of transistor Q5 switches from positive to ground and continues to oscillate until integrated circuit IC15 output pin 6 returns to a ground potential. Upon receipt of the second output cycle of the oscillator, integrated circuit IC16 divides the frequency by a factor of two. This output is routed from pin 12 to integrated circuit IC16 pin 5 and IC17 pin 1. The input being applied to integrated circuit IC16 pin 5 is not divided again because the ground potential that is present at input pin 6

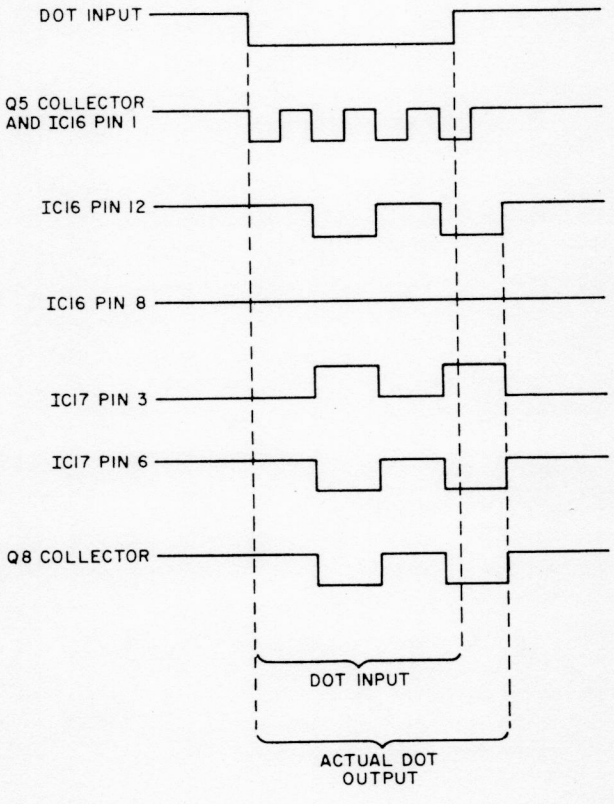


Figure 3-12. "DOT" Generation Timing Diagram

is holding the output at pin 8 at a constant positive potential. Whenever a ground potential from integrated circuit IC16 output pin 12 is applied to integrated circuit IC17 input pin 1 it drives the output at pin 3 to a positive potential which in turn drives the output at integrated circuit IC17 pin 6 to a ground potential. The output from pin 6 is routed to integrated circuit IC15 pin 4 and also to the base of transistor Q8. The ground potential forward biases transistor Q8 causing its collector potential to switch to a ground potential that is used as a "DOT" output at Counter board output pin 361. A recycling of events will occur as long as the "DOT" input to integrated circuit IC15 pin 1 is grounded. If the "DOT" input is removed during the time when a "DOT" ground output is present, the output state of integrated circuit IC17 pin 6, that is being applied to IC15 input pin 4, holds the output at IC15 pin 6 at a positive potential. Thus transistor Q8 remains operational until the newly generated "DOT" output is completed. The description given for the "DOT" condition is pictorially depicted by the timing diagram shown in Figure 3-12.

In a "DASH" condition, a ground is routed from an external speed key to rear panel "KEYER" connector J12 pin 1, then to Counter board input pin 360 and is applied to integrated circuit IC15 pin 2 driving the output at pin 6 to a positive potential. The operation of the multivibrator is enabled as previously described in the "DOT" condition explanation. The "DASH" input ground is also applied to integrated circuit IC17 input pin 12 which causes output pin 11 to switch to a positive potential. This permits the second divide-by-two circuit to be operational. The multivibrator oscillator output that has been divided by two, at integrated circuit IC16 output pin 12, is applied to integrated circuit IC16 input pin 5 and is then divided by two again. The output from integrated circuit IC16 pin 8 is applied to integrated circuit IC17 input pin 13 and IC17 input pin 2. If the "DASH" input is removed during the time when the "DASH" ground output is present, the ground potential from integrated circuit IC16 output pin 8, that is being applied to integrated circuit IC17 input pin 13, holds the output at IC17 pin 11 at a positive potential. Thus, the output from integrated circuit IC17 pin 11 is not permitted to inhibit the operation of the second divide-by-two circuit until the output "DASH" cycle is completed. Both divider outputs are applied to integrated circuit IC17 input pins 1 and 2 respectively. It is the gating action of this integrated circuit that makes the dash output exactly three times the length of the dot output. The outputs of both dividers are 180° out-of-phase with each other and the combined ground

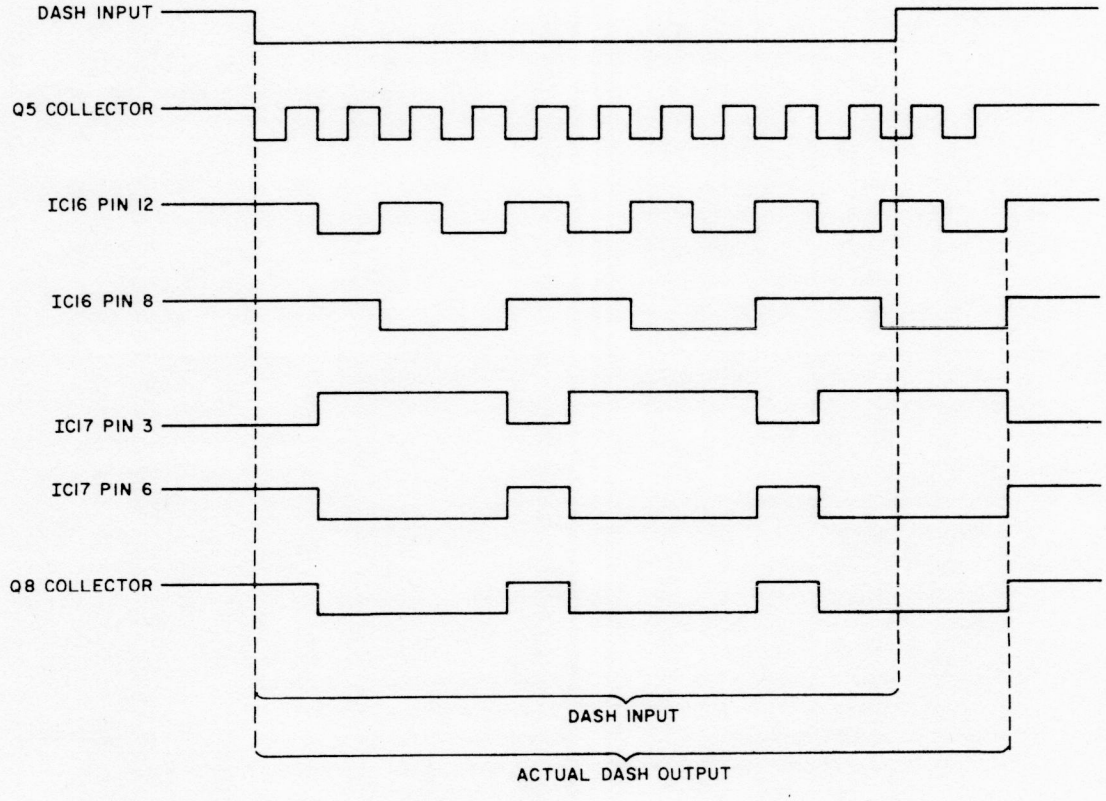


Figure 3-13. "DASH" Generation Timing Diagram

potential being applied to integrated circuit IC17 input pins 1 and 2 drives the output at pin 3 to a positive potential. This output is processed through the keyer circuitry in the same manner as previously described for a "DOT" condition.

The description given for the "DASH" condition is pictorially depicted by the timing diagram shown in Figure 3-13.

3.3 RECEIVER CIRCUITRY

A stage-by-stage receive signal path diagram is shown in Figure 3-14. Unless otherwise indicated in the following explanation, it is assumed that the CX7 is operating in the single sideband mode with the front panel "AGC" switch set to "OFF."

3.3.1 Receive Signal Path

RF signals from the main antenna connector J15, located on the CX7 rear panel, are routed through the PA Assembly reed relay K1 deenergized contacts 18 and 11 to the swinger of the "AUX-COM" switch S9 located on the CX7 rear panel. This switch must be set to the "COM" position if it is desired to receive and transmit using the same antenna. The RF signal from the switch is routed to PA Assembly output connector J14 and then to the input of the High Pass Filter board. The filter prevents commercial broadcast crossmodulation interference from entering the receiver. The RF signal from the High Pass Filter board output pin 521 is connected to the Front End board input pin 76. The level of the RF signal at this point is approximately 0.3 microvolt or more within the 1 to 30 MHz frequency range. The RF signal from input pin 76 is coupled through tuned circuits to gate G1 of dual gate field effect transistor Q1. Gate G2 of transistor Q1 would normally receive an AGC control voltage. Transistor Q1 functions as a highly linear, low noise RF amplifier of wide dynamic range. The output of transistor Q1 is coupled to gate G1 of dual gate field effect transistor Q2. Gate G2 of transistor Q2 is receiving a mixing frequency (being determined by the setting of the front panel "MHZ" selector switch S7) which is generated by the crystal oscillator transistor Q7 and routed through buffer transistor Q6, Front End board output pin 53 and input pin 71. The RF signal and the local oscillator frequency are mixed by transistor Q2 to produce a resultant difference frequency in the range of 39 to 40 MHz. The mixer output is coupled through tuned circuits to gate G1 of dual gate field effect transistor Q3. Gate G2 of transistor Q3 also normally receives an AGC voltage. Transistor Q3 functions as an RF amplifier and its output is coupled through a tuned circuit to Front End board output pin 68. The RF level at output pin 68 is approximately 150 millivolts, RMS at a frequency of 39 to 40 MHz.

The Front End board output pin 68 is connected to IF board input pin 421 and coupled through a tuned circuit to gate G1 of dual gate field effect transistor Q10. Gate G2 of transistor Q10 is receiving a mixing frequency in the range of 30.1 to 31.1 MHz which originates in the mixer stages that are explained in paragraph 3.4.4. The 39 to 40 MHz and the 30.1 to 31.1 MHz frequencies are mixed by transistor Q10 to produce a resultant difference frequency that is exactly 8.815 MHz. The mixer output is routed through a 25 kHz bandpass filter FL3 and coupled to gate G1 of dual gate field effect transistor Q11. Gate G2 of transistor Q11 has a constant fixed bias applied and receives no input, control or command signal. The output of transistor Q11 is applied to the signal input of the noise blanker gate (a detailed explanation of the noise blanking method is given in paragraph 3.3.2). The output of the noise blanker gate is processed through filter FL1, to limit its bandwidth to 2.4 kHz, and is applied to integrated circuit IC3 functioning as a linear amplifier. The signal is then further conditioned by an additional 2.4 kHz bandpass filter FL2 and applied to integrated circuit IC4, also functioning as a linear amplifier. Both integrated circuits IC3 and IC4 receive normal and delayed AGC voltages. The output signal from integrated circuit IC4 is routed through emitter follower transistor Q16 to IF board output pin 465. The nominal level of the 8.8 MHz signal at output pin 465 is 30 millivolts, RMS.

The output from the IF board is connected to AGC Detector board input pin 493 and then coupled to the input of integrated circuit IC1 functioning as a linear amplifier. The output of integrated circuit IC1 drives two different circuits. One is the AGC circuitry, discussed in paragraph 3.3.3 and the other is the product detector transistor Q6. Gate G1 of dual gate field effect transistor Q6 receives the 8.8 MHz sideband signal from integrated circuit IC1 and gate G2 receives an 8.8 MHz carrier frequency via AGC Detector board input pin 487 and BFO board output pin 215. The detected output of transistor Q6 is coupled to AGC Detector board input pin 485. The level of the audio signal is within an approximate range of 50 to 150 millivolts, RMS and is applied to the front panel "AF-GAIN" potentiometer R14.

The audio signal from the wiper of potentiometer R14 is routed to Audio board input pin 308 and is coupled to the gate of field effect transistor Q9. The amplified output from transistor Q9 is passed through the normally enabled field effect transistor Q18, functioning as an audio gate (Q18 is inhibited in the transmit mode) and is amplified by field effect transistor Q19. The output of transistor Q19 is connected to Audio board output pin 313.

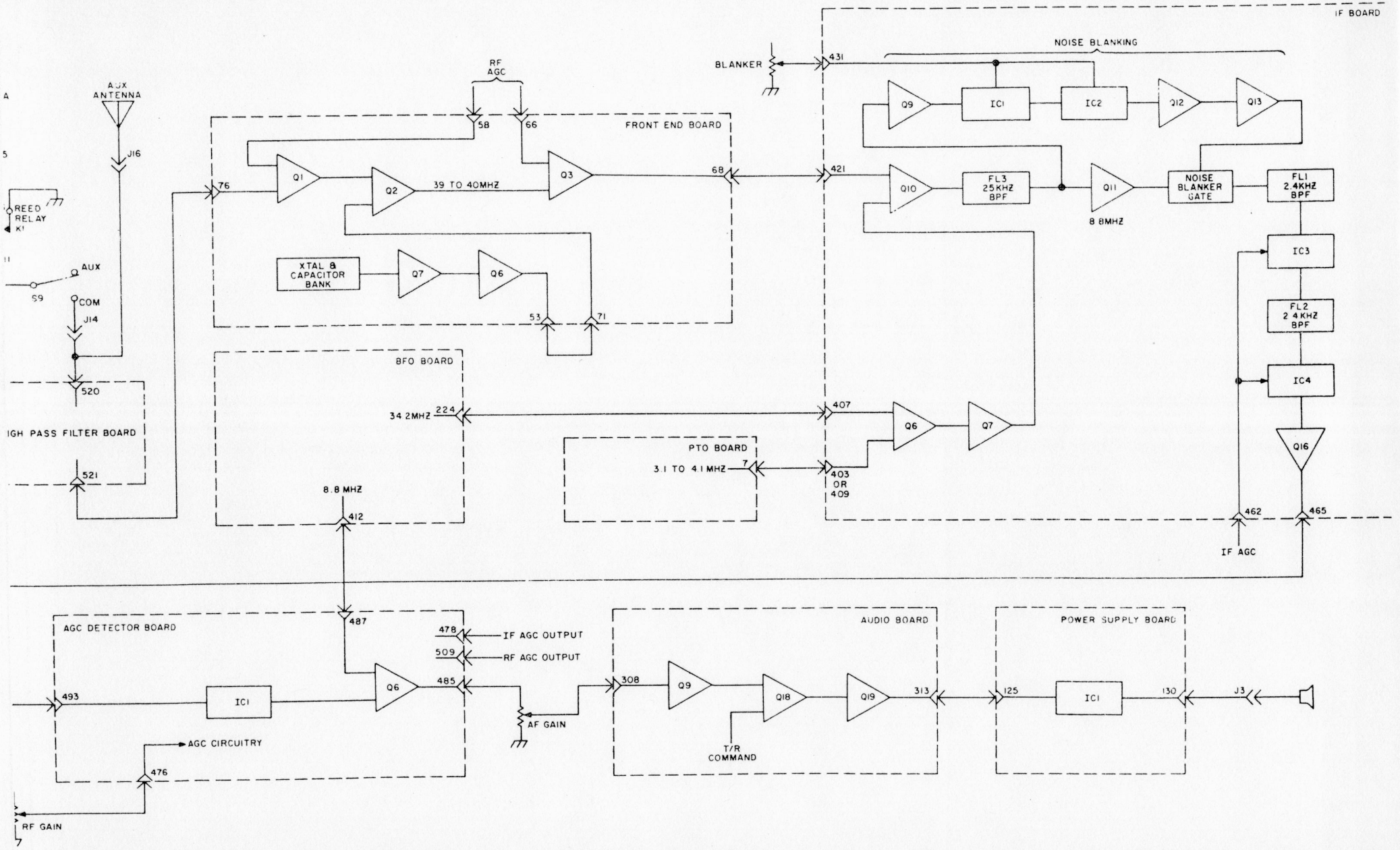


Figure 3-14. Receive Signal Path Block Diagram

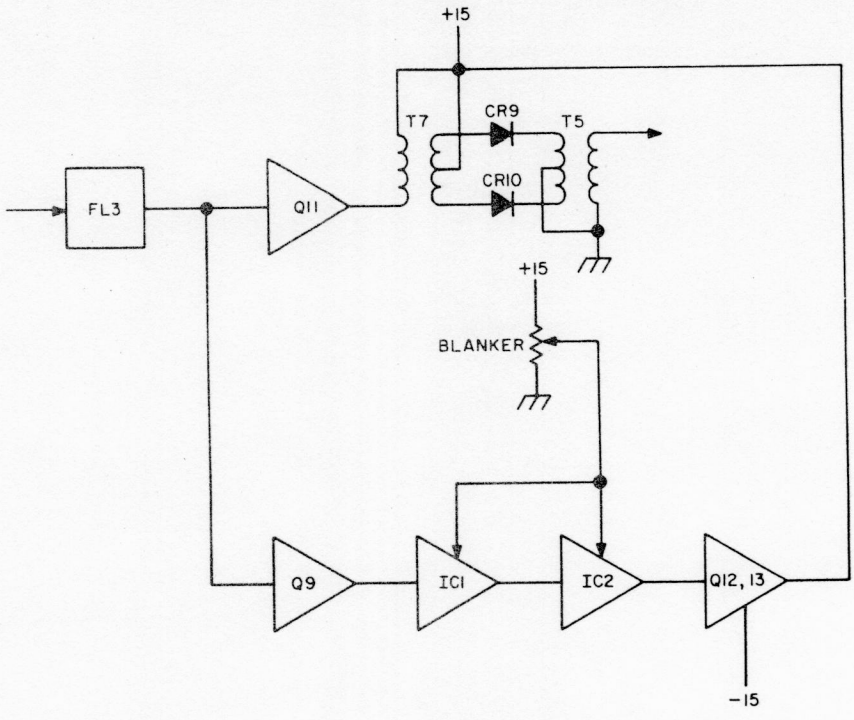


Figure 3-15. Noise Blanker Simplified Schematic Diagram

The signal from the Audio board is connected to Power Supply board input pin 125 and is then applied to integrated circuit IC1 functioning as a linear audio amplifier. The audio output of integrated circuit IC1 is connected to Power Supply board output pin 130 and then routed to the primary of audio output transformer T2, located on the inside rear panel. The secondary of transformer T2 is connected to the front panel "PHONES" connector J1 and the rear panel "SPKR" connector J3. Connectors J1 and J3 are interwired so that the speaker output is interrupted whenever the headphones are connected. Transformer T2 also provides a 600-ohm output to "POWER" connector J6 pins 4 and 5.

3.3.2 Noise Blanker

The noise blanker circuit is utilized by the CX7 to inhibit the received signal from passing through the 8.8 MHz IF stage during the presence of strong RF noise pulses. The operation of the circuit can be manually adjusted by the front panel "NOISE BLANKER" control. A simplified diagram of the noise blanker circuit is shown in Figure 3-15.

The noise blanker circuit is located on the IF board. The 8.8 MHz IF output of bandpass filter FL3 is connected to the gate of field effect transistors Q9 and Q11. The IF signal is amplified by transistor Q11 and is then applied to the primary of transformer T7. The noise blanker gate is comprised of transformers T5 and T7, and diodes CR9 and CR10. When the "NOISE BLANKER" potentiometer R5 on the CX7 front panel is in the "OFF" position, or when no RF noise pulses are present, the Darlington connected transistor detectors Q12 and Q13 are nonconducting. This permits diodes CR9 and CR10 in the noise blanker gate to be forward biased and pass the IF signal. Field effect transistor Q9, integrated circuits IC1 and IC2 along with the Darlington transistor pair Q12 and Q13 comprise an 8.8 MHz noise amplifier. The gain of integrated circuits IC1 and IC2 is controlled by potentiometer R5. When noise pulses are present, they are amplified to an amount sufficient enough to forward bias the base of Darlington connected transistors which, in turn, provides a negative potential that reverse biases diodes CR9 and CR10. Whenever these diodes are reverse biased, the 8.8 MHz IF signal is effectively blocked by the noise blanker gate for the duration of the RF noise pulse.

3.3.3 Automatic Gain Control

The automatic gain control (AGC) is employed by the CX7 to maintain a constant receive signal level passing through the Front End and IF boards. The AGC circuitry can be completely disabled by switching the front panel "AGC" control to the "OFF" position. A simplified diagram of the AGC circuit and the circuitry it controls is shown in Figure 3-16.

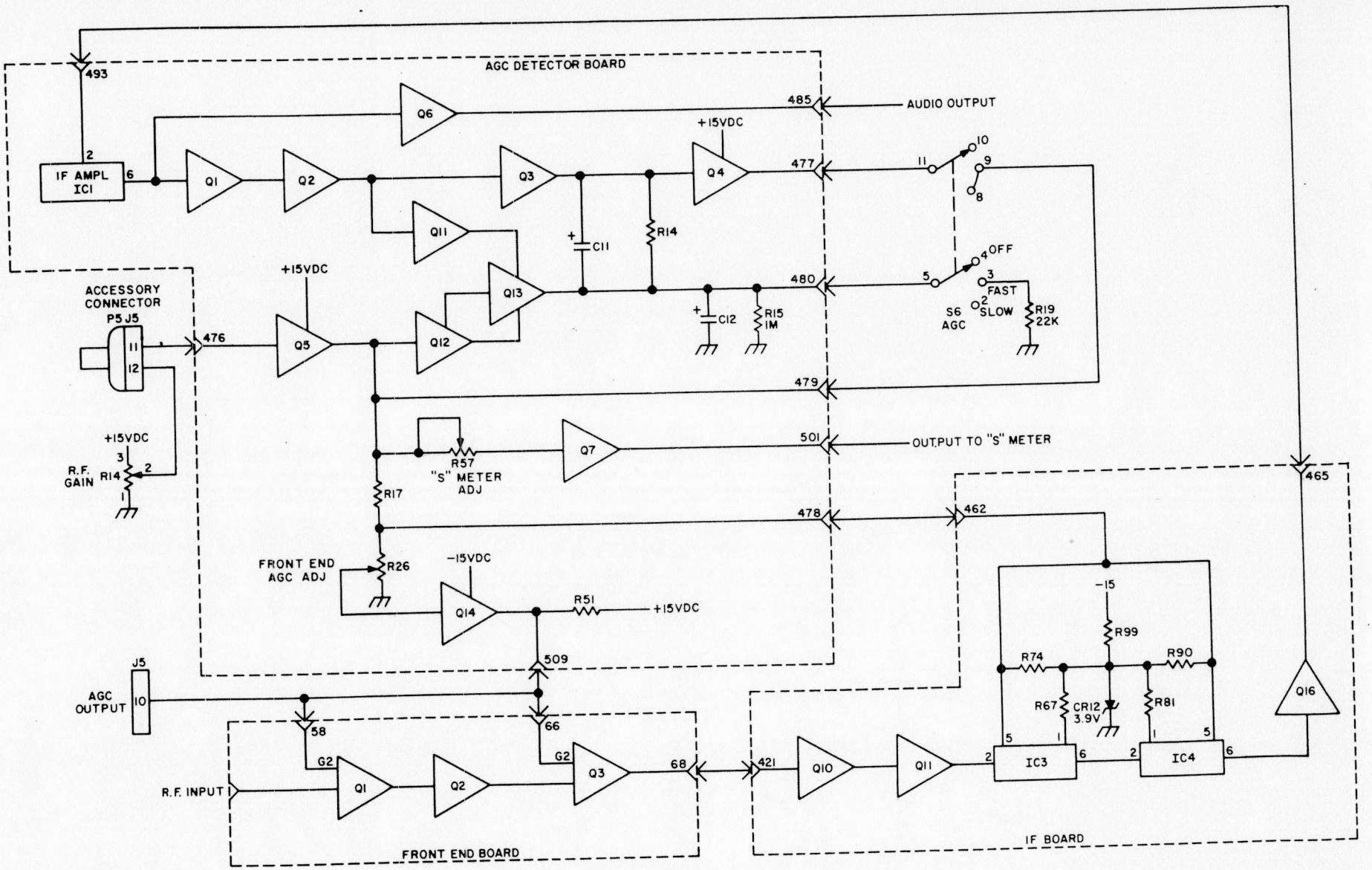


Figure 3-16. Automatic Gain Control Simplified Schematic Diagram

The AGC circuit is located on the AGC Detector board. Its controlling effects can be overridden by setting of the front panel "RF GAIN" potentiometer R14. The AGC circuit provides two primary outputs with an increasing RF input signal level. First, the AGC voltage to the Front End board should be increasing in negative direction. Second, the AGC voltage to the IF board should be increasing in positive direction.

With the front panel "AGC" switch S6 set to the "OFF" position, the front panel "RF GAIN" potentiometer R14 still can control the gain in the Front End and IF boards. A positive potential from the wiper of potentiometer R14 is routed through rear panel connector J5 (accessory connector) pins 11 and 12 to the AGC Detector board input pin 476 and then to the base of transistor Q5 as bias. The amount of positive potential selected by the wiper of potentiometer R14 determines the conduction rate of transistor Q5. Resistors R17 and R26 form a voltage divider operating from the emitter current of transistor Q5. Consequently, the emitter current is responsible for developing the potential to forward bias the base of transistor Q14 and the control bias for integrated circuits IC3 and IC4 to reduce the gain in the RF signal path stages. The conduction of transistor Q14 provides a negative potential that is routed to AGC Detector board output pin 509 and Front End board input pins 58 and 66. The negative potential is utilized to decrease the gain of dual gate field effect transistors Q1 and Q3 on the Front End board. When the potential reaches -0.5 VDC, the transistors are cut off. This AGC voltage is also routed to the rear panel connector J5 pin 10 for auxiliary equipment use.

The positive voltage potential that is present at the junction of resistors R17 and R26 is routed to AGC Detector board output pin 478 and IF board input pin 462. The positive potential provides control bias for integrated circuit IC3 pin 1 and IC4 pin 1. The voltage must be more positive than -3.9 VDC in order to take precedence over the negative voltage developed by Zener diode CR12. If the potential being applied to IF board input pin 462 becomes more positive, the signal output of the integrated circuits decreases. When the potential reaches +3.0 VDC, the integrated circuits are cut off.

The AGC circuit is comprised of transistors Q3, Q4, Q11, Q12, and Q13. When the front panel "AGC" switch is positioned to either "FAST" or "SLOW" and the setting of the "RF GAIN" control is not forward biasing the base of transistor Q5, the emitter current of transistor Q4 must establish the voltage potential at the junction of resistors R17 and R26. Under a no RF signal input condition, transistors Q2 through Q4 are reverse biased permitting the RF signal path stages to operate at maximum gain. With an RF signal present, the same processed receive signal being applied to the input of the product detector is also applied to the input of the AGC amplifier transistor Q1. Transistor Q2 functions as an AGC detector. When the amplified output of transistor Q1 is sufficient enough to forward bias the base of transistor Q2, it conducts, causing transistors Q3 and Q11 to also be forward biased. Capacitors C11 and C12 are permitted to charge at this time which in turn provides forward bias for the base of transistor Q4. The emitter current of transistor Q4 is routed through voltage divider resistors R17 and R26. Consequently, the emitter current is responsible for developing the potential to forward bias the Darlington connected transistors Q12 and Q13. However, the emitter of transistor Q13 is being reverse biased by the conduction of transistor Q11. When the received signal decreases sufficiently to permit the base of transistor Q2 to become reverse biased, transistors Q2 and Q11 immediately switch to an "OFF" condition. During this process, transistor Q14 conduction decreases slowly while capacitors C11 and C12 discharge, but then rapidly due to the action of transistors Q12 and Q13 aiding the discharge by momentarily switching to an "ON" condition.

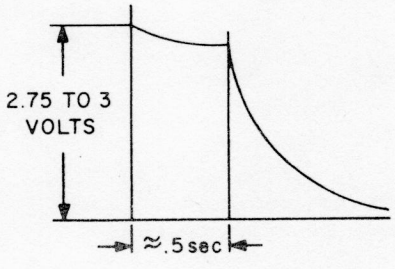


Figure 3-17. "SLOW" AGC Voltage Curve

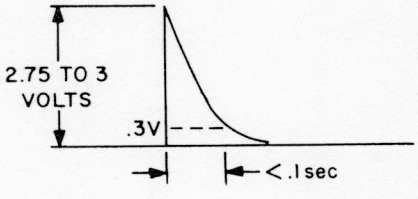


Figure 3-18. "FAST" AGC Voltage Curve

With the "AGC" switch S6 in the "SLOW" position, the resultant AGC voltage curve, as measured at the AGC Detector board output pin 478, is shown in Figure 3-17. With the "AGC" switch S6 in the "FAST" position, resistor R22 increases the discharge time of capacitor C12 as shown in Figure 3-18.

Transistor Q7 functions as a meter amplifier and inverts the AGC voltage producing an output that is relative to the received signal strength.

3.3.4 Receiver Enabling

Receiver enabling is defined as satisfying the prerequisit conditions that must be present in order for the RF signal to be processed through the receive circuitry. If any external source is not supplying a ground to key the transmit circuitry and the front panel "PTT" switch is depressed, the CX7 is automatically in the receive mode. The command signals for receive enabling are generated by the same circuits previously explained in paragraph 3.2.4. However, the input and output state of the applicable transistors are just the opposite for a receive condition.

The CX7 utilizes ANTI-VOX circuitry to ensure that a receive condition is maintained and not changed by speaker noise. A simplified diagram of the ANTI-VOX circuitry is included in the VOX keying diagram shown in Figure 3-8.

The rear panel "ANTI-TRIP" potentiometer R11 is connected across the audio output transformer T2 terminals 1 and 2. Any audio that is present at the speaker is routed from the wiper of R11 to Audio board input pin 320 and coupled to the base of transistor Q10. The amplified output of transistor Q10 is coupled to the base of emitter follower transistor Q11 which has its output direct-coupled to the base of transistor Q12. If the ANTI-VOX audio signal is strong enough, it causes transistor Q12 to switch to an "OFF" condition which, in turn, causes the following transistors to switch to the indicated state:

Transistor	Output State
Q13	OFF
Q14	OFF
Q15	ON
Q16	ON
Q17	OFF

As shown in Figure 3-8, both "VOX" and "ANTI-VOX" signals are applied to the base of switching transistor Q12. The input levels of each signal is adjustable; consequently, the strongest signal will take precedence in determining the resultant base bias of transistor Q12. Under normal operation, the "VOX" signal is usually adjusted to have the larger signal.

3.4 FREQUENCY MIXING NETWORK

This network consists of various oscillators located on the BFO board, two separate PTO modules (VFO), and mixer stages located on the IF board. VFO and BFO signals are processed on the IF board. Front panel controls influencing this network operation include the VFO-A, VFO-B, TRANSMIT-A/T.O., TRANSMIT-A, TRANSMIT-B, SPOT, IF SHIFT, TRANSMITTER OFFSET, RECEIVE CHANNEL SELECTOR, RECEIVE CHANNEL BALANCE, CALIBRATOR, and MODE.

The objective of this mixing network in the transmit mode is to provide a frequency that is utilized for translating the 8.8 MHz SSB to the 39 to 40 MHz transmit IF. The Front End board provides conversion to the actual transmit frequency. While in the receive mode, the objective of this mixer network is to provide a frequency utilized for translating the 39 to 40 MHz receive IF to the 8.8 MHz receive IF and also provides such features as IF Shift, Calibration, and upper and lower sideband functions. In both sideband modes, the VFO provides the means for bandspread tuning.

The basic concept of this frequency mixing network employed by the CX7 is shown in Figure 3-19. The 34.2 MHz source is variable to a slight degree but for preliminary explanation purposes, it is shown as being fixed. The 34.2 MHz frequency is mixed with the VFO oscillator that is tunable throughout the range of 3.1 and 4.1 MHz. The resultant difference output frequency of this mixer is dependent upon the setting of the tunable oscillator and will be in the range of 30.1 and 31.1 MHz. The frequency is mixed with the transmit 8.8 MHz SSB input by transistor Q8 to produce the sum frequency in the range of 39 to 40 MHz. As previously discussed in the transmit signal path explanation, the 39 to 40 MHz IF is further converted by a mixer on the Front End board to the actual transmit output frequency. Bandspread tuning is accomplished solely by tuning the 3.1 to 4.1 MHz VFO oscillator.

In the basic frequency concept explanation, only one 34.2 MHz source and one tunable source feeding a common mixer was utilized. The actual CX7 circuitry employs the use of two 34.2 MHz sources, two tunable sources feeding three separate mixers in order to facilitate dual receive and transmit offset functions. The following paragraphs cover the operation of the PTO, individual oscillators on the BFO board and their interconnections with the mixers.

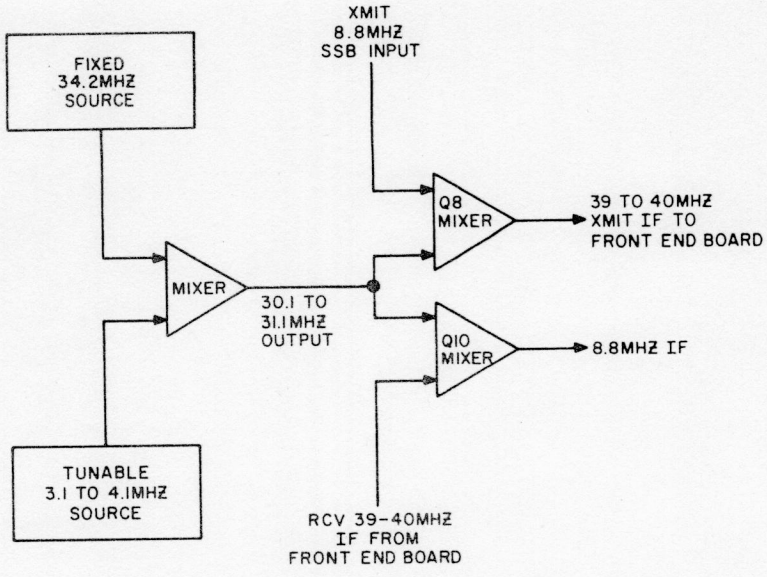


Figure 3-19. Simplified Frequency Mixing Network Block Diagram

3.4.1 Permeability Tuned Oscillators

The 3.1 to 4.1 MHz tunable source utilized by the CX7 is the permeability tuned oscillator (PTO). Figure 3-20 is a simplified block diagram of the PTO. Field effect transistor Q1 and its associated circuitry function as a Colpitts oscillator. The tuned circuit output is rectified by diode CR1 and is used to provide gate bias for transistor Q1. The inductance of inductor L1 is changed by tuning the applicable front panel "VFO-A" or "VFO-B" control. The output of transistor Q1 is routed through buffer transistor Q2 and emitter follower transistor Q3 to PTO board output pin 7. The PTO is enabled or inhibited by switching the gate bias supply of transistor Q1 along with the collector supply of transistors Q2 and Q3. A ground applied to PTO board input pin 4 enables the PTO. A zero or -15 VDC potential applied to pin 4 is utilized to inhibit the operation of the PTO. In PTO A, varactor CR2 is permanently reverse biased by -15 VDC being applied to PTO A board input pin 1, therefore its capacitance does not influence the tuned circuit frequency. In the "FSK" mode, the negative potential being applied to PTO B input 1 can be reduced by the front panel "FSK SHIFT" potentiometer R1. This causes the capacitance change of varactor CR2 to change the tuned circuit frequency up to one kHz.

3.4.2 Normal 34.2 MHz Source

The 34.2 MHz source is also variable permitting the following functions to be accomplished: IF shift, upper and lower sideband frequency generation, and calibration. A simplified diagram of the 34.2 MHz source is shown in Figure 3-21. The 34.2 MHz is obtained by mixing 8.8 MHz and 43.1 MHz and using the resultant difference. The circuitry is located on the BFO board. The IF shift and upper and lower sideband selection is accomplished by changing the characteristics of the 8.8 MHz oscillator. In the AM, FSK, CW or USB mode, the "MODE" switch S8B routes -15 VDC to BFO board input pin 216 and it is then applied to diodes CR4 and CR5. The negative potential forward biases diode CR5 and reverse biases diode CR4 permitting the 8.8165 MHz crystal Y2 to determine the basic frequency of the oscillator integrated circuit IC1. If the "MODE" switch S8B was in the "LSB" position, a positive potential would be applied to forward bias diode CR4 and reverse bias CR5 permitting the 8.8135 MHz crystal Y1 to determine the basic frequency of the oscillator integrated circuit IC1. In the transmit mode transistor Q1 is "ON" and transistor Q2 is "OFF" because T/R commands are applied to their base junctions, therefore the front panel "IF SHIFT" control setting has no effect upon the varactor CR1. In the receive mode, transistor Q1 is "OFF" and transistor Q2 is "ON." (A +0.3 VDC potential is routed from Audio board output pin 326, through the deenergized "SPOT" switch S2E contacts 16 and 17 to BFO board input pin 219 and then to the base of transistor Q1. A -13.5 VDC potential is also routed from Audio board output pin 327, through the deenergized "SPOT" switch S2E contacts 1 and 2 to BFO board input pin 221 and then to the base of transistor Q2.) The front panel "IF SHIFT" potentiometer R6 is connected to the BFO board via input pins 217, 218, and 222. In the receive mode the biasing of transistors Q1 and Q2 provide a negative potential that is routed from the wiper of "IF SHIFT" potentiometer R6 and is then applied to varactor

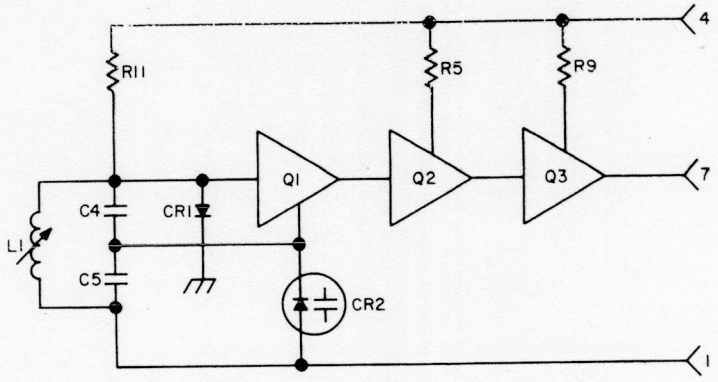


Figure 3-20. PTO Simplified Schematic Diagram

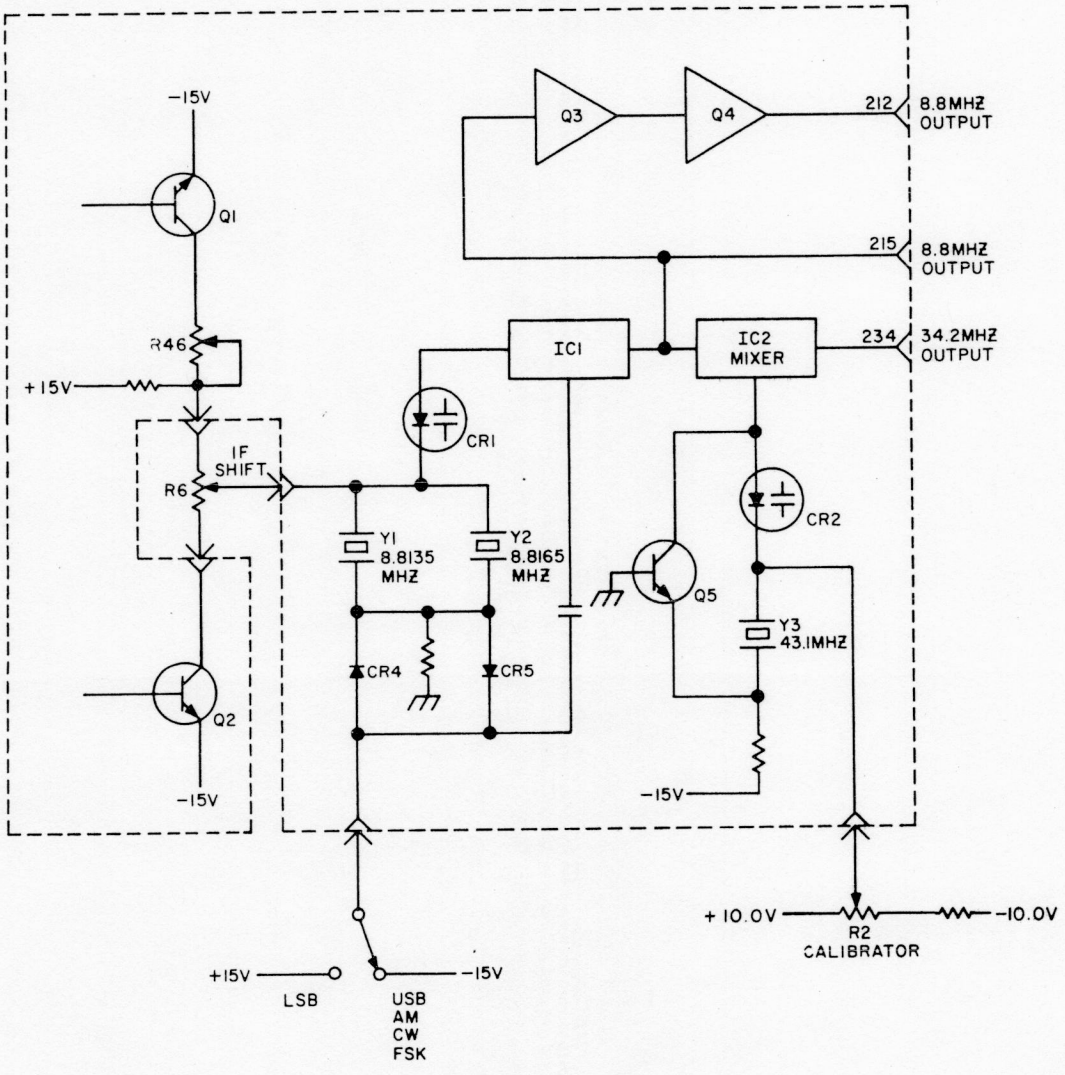


Figure 3-21. Normal 34.2 MHz Oscillator Simplified Schematic Diagram

CR1. The setting of potentiometer R6 determines the bias of varactor CR1 causing its capacitance change to shift the 8.8 MHz oscillator frequency by a specific amount in the range of ±1.6 kHz from the selected sideband frequency. This permits an unwanted receive frequency to be shifted outside of the bandpass of the IF board filters. The 8.8 MHz oscillator provides three different outputs. One output is coupled to buffer amplifier transistor Q3. The output of transistor Q3 is coupled to emitter follower transistor Q4 and its output is routed to the BFO board output pin 212 and then to the AGC Detector board input pin 495. This 8.8 MHz frequency is utilized by the AGC Detector board balanced modulator and single sideband gate circuitry. The second output of the 8.8 MHz oscillator is routed directly to the AGC Detector board product detector circuit via BFO board output pin 215 and AGC Detector board input pin 487. The third output of the 8.8 MHz oscillator is coupled to integrated circuit mixer IC2.

The 43.1 MHz oscillator is comprised of transistor Q5, 43.1 MHz crystal Y3, and varactor diode CR2. This circuitry is also located on the BFO board. A negative potential from the wiper of the front panel "CALIBRATOR" potentiometer R2 is routed to diode CR2 via BFO board input pin 202. The setting of potentiometer R2 determines the bias of diode CR2 causing its capacitance change to shift the overall 43.1 MHz oscillator frequency by a specific amount in the range of ±1.5 kHz. This permits errors in the Front End board local oscillator crystals to be corrected.

3.4.3 Offset 34.2 MHz Oscillator

The offset 34.2 MHz oscillator is only utilized in the transmit mode. It has a wider variable range than the 34.2 MHz source previously discussed. A simplified diagram of the offset 34.2 MHz oscillator is shown in Figure 3-22. The oscillator frequency is determined by the 11.4278 MHz crystal Y4 and the setting of the front panel "TRANSMITTER OFFSET" potentiometer R8. Integrated circuit IC3 functions as an oscillator. The output tuned circuit selects the third harmonic of 34.2 MHz. The entire circuit functions as an oscillator and tripler; consequently, the forward bias of varactor diode CR3 can change the output frequency by as much as ±3 kHz. The 34.2 kHz frequency is routed to BFO board output pin 207 and then to IF board input pin 405.

3.4.4 VFO Mixers

The VFO associated mixers are dual gate field effect transistors located on the IF board. A simplified diagram of these mixers is shown in Figure 3-23. Transistors Q4 and Q5 function as spotting mixers providing an audio output frequency that is the resultant difference between the two RF inputs. Transistors Q2, Q3, and Q6 also operate as difference mixers providing a 30.1 to 31.1 MHz output and independently function identically as the 30.1 to 31.1 MHz mixer discussed in the basic CX7 VFO concept. Transistors Q1 and Q7 function as buffer amplifiers. The transmit mixer transistor Q8 and the receive mixer transistor Q10 are also the same transistors that were discussed in the basic VFO concept. During the dual receive mode, transistors Q3 and Q6 are the only mixers that are utilized at the same time and in all other modes, transistors Q2 through Q6 are only used one at a time for their specific function. The mixer transistors are enabled and inhibited by switching the potentials applied to the gate G2 lead resistor. A zero VDC or ground potential enables the mixer and a -15 VDC potential inhibits the mixer. The commands are routed through the "TRANSMIT VFO-A", "TRANSMIT VFO-B", "TRANSMIT VFO-A/T.O.", "SPOT", and "RECEIVE CHANNEL" switches.

Figure 3-24 shows how the mixers and oscillators are interconnected through the network of switches. Table 3-1 is provided for a quick reference to determine what stages are being enabled and inhibited for various switch positions. Mixer transistor Q5 is enabled only when the "SPOT" switch is depressed and provides an audio output when the difference between the two PTO output frequencies is in the audio range. Mixer transistor Q4 is only enabled when the "SPOT" switch is depressed and the "TRANSMIT VFO-A/T.O." switch is energized. Transistor Q4 provides an audio output when the difference between the two 34.2 MHz frequencies is in the audio range. The output of transistors Q5 and Q4 is routed to IF board output pin 413 and then to the front panel "SPOT LEVEL" potentiometer R3. The signal from the wiper of potentiometer R3 is routed to Audio board input pin 310 and then coupled into the audio amplifier circuitry. Mixer transistor Q2 only functions in the transmit mode and receives an RF input from the 34.2 MHz offset oscillator and PTO A. Transistor Q2 is only enabled by a T/R command during a transmit condition when the "TRANSMIT VFO-A/T.O." switch is energized. Mixer transistor Q3 receives RF inputs from the normal 34.2 MHz source and PTO A.

When the front panel "RECEIVE CHANNEL" switch S5B is set to the "DUAL" position and the front panel receive balance potentiometer R7 is centered in its range, mixer transistors Q3 and Q6 are both enabled. This biasing condition permits the CX7 to process the demodulation of two separate signals. The 34.2 MHz frequency signal level being applied to transistors Q3 and Q6 remains the same. The transistor itself is cut off by the application of proper DC logic to gate 2.

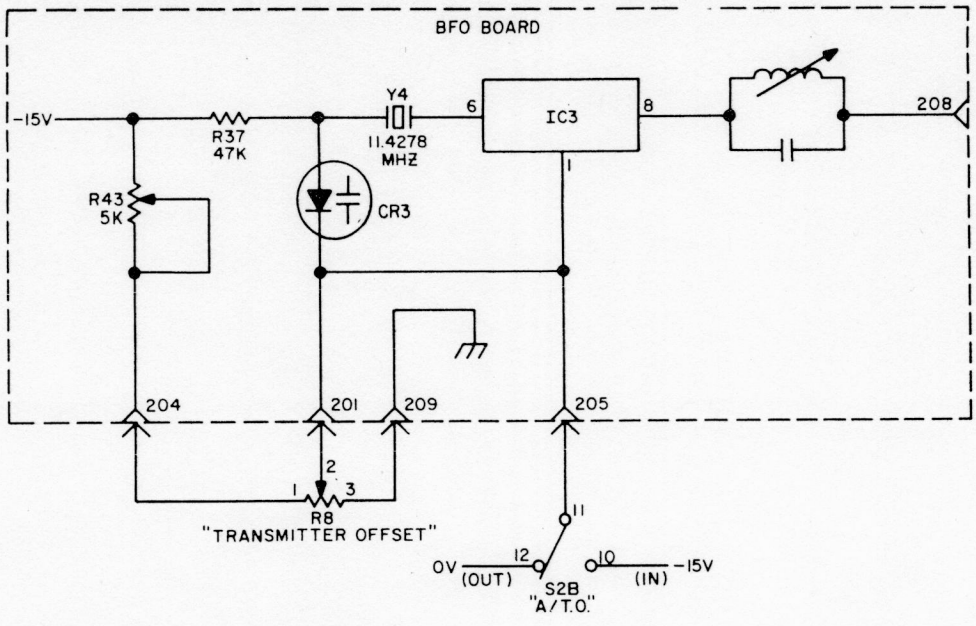


Figure 3-22. Offset 34.2 MHz Oscillator Simplified Schematic Diagram

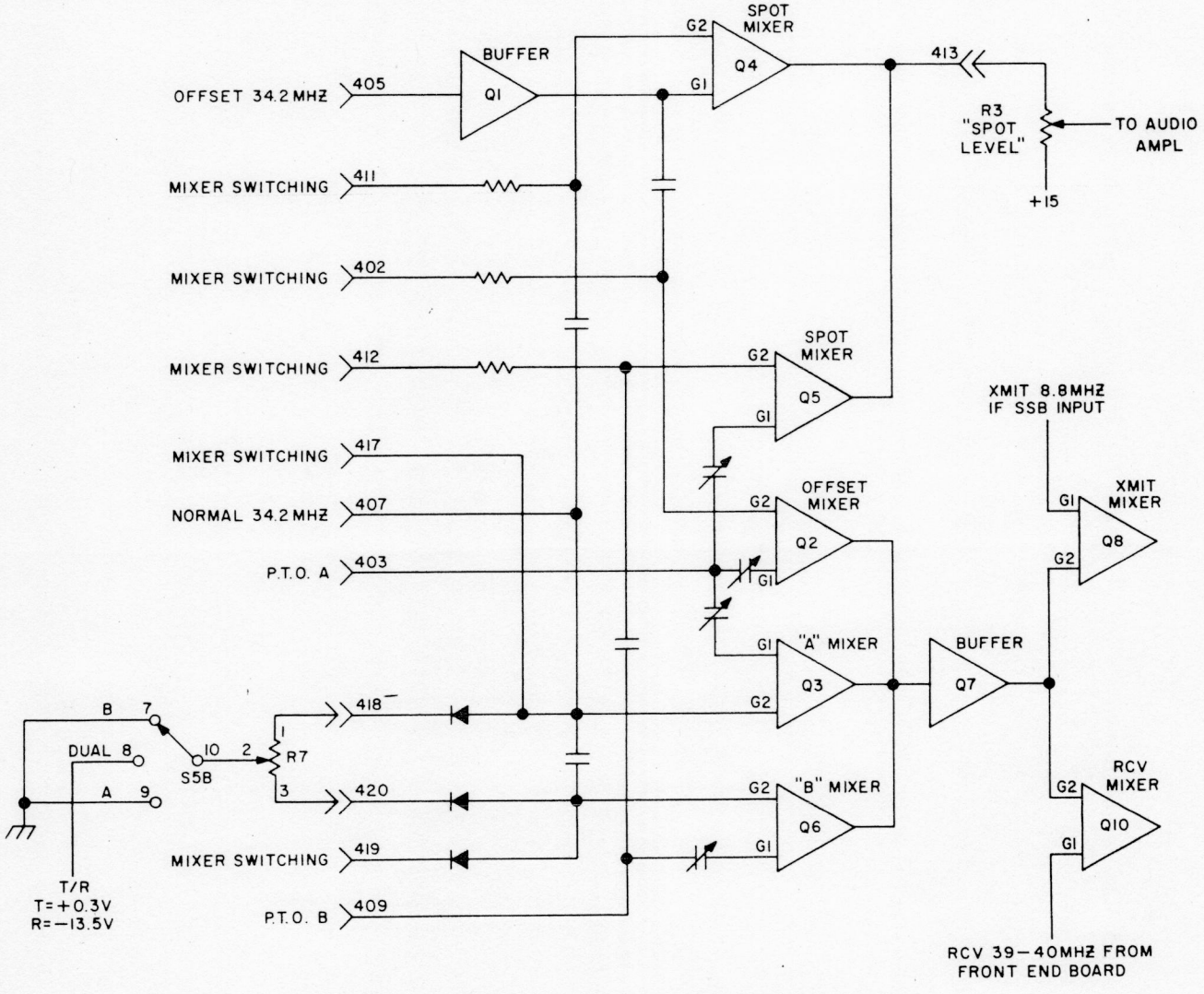


Figure 3-23. VFO Mixer Simplified Schematic Diagram

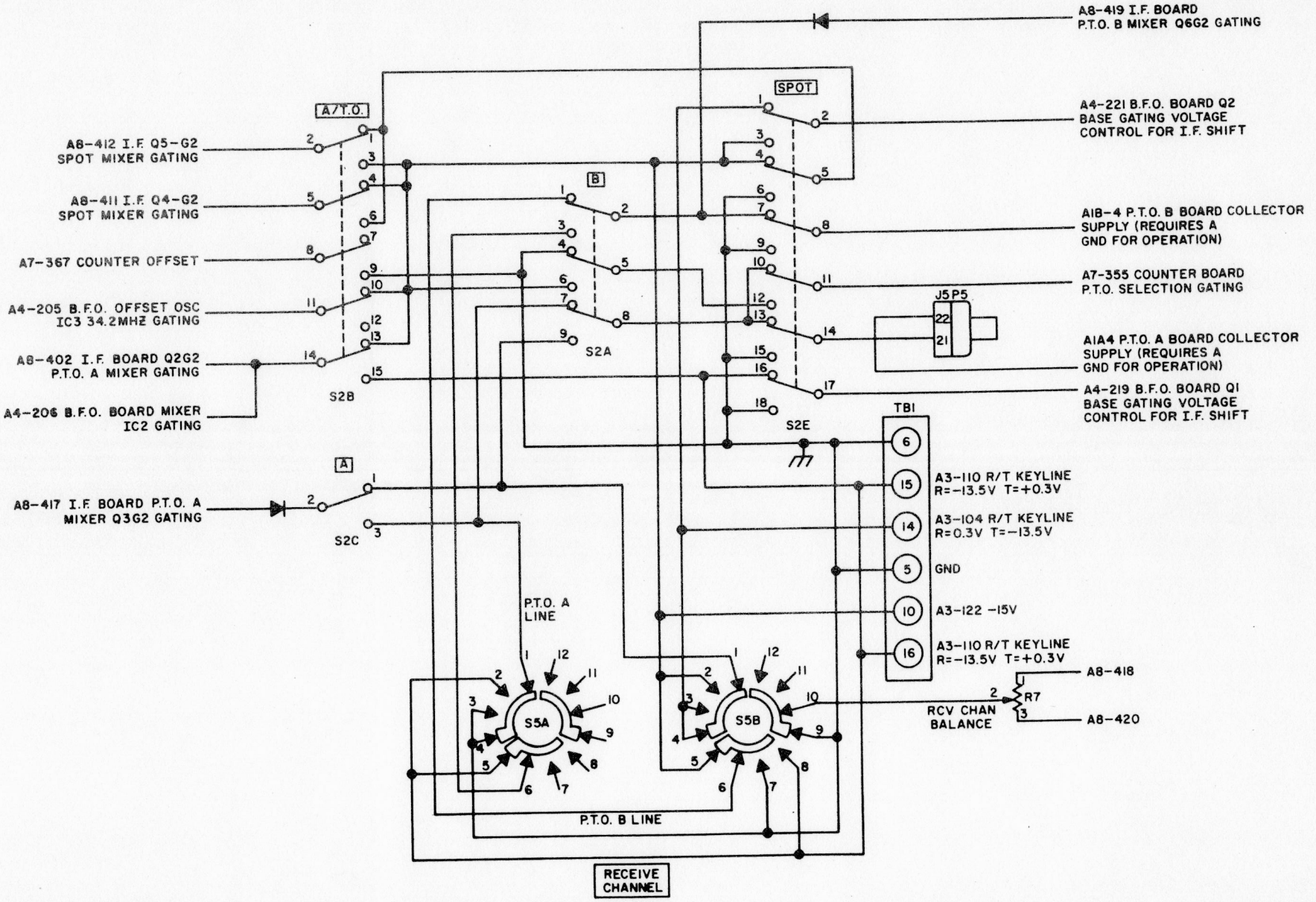


Figure 3-24. VFO Control Switching Simplified Schematic Diagram

SWITCH STATUS						COMMAND RECEIVED						
ITEM NO.	RECEIVE CHANNEL (S5)	TRANSMIT–VFO A (S2C)	TRANSMIT–VFO B (S2A)	TRANSMIT–VFO A/T.O. (S2B)	SPOT (S2E)	OFFSET MIXER (Q2)	B MIXER (Q6)	B PTO (PIN 4)	A MIXER (Q3)	A PTO (PIN 4)	A/B MIXER (Q5)	34.2 MHz MIXER (Q4)
1	A	OUT	OUT	OUT	OUT	-15V	-15V	-15V	R/T	GRD	-15V	-15V
2	A	IN	OUT	OUT	OUT	-15V	-15V	-15V	GRD	GRD	-15V	-15V
3	A	OUT	IN	OUT	OUT	-15V	T/R	T/R	R/T	R/T	-15V	-15V
4	A	OUT	OUT	IN	OUT	T/R	-15V	-15V	R/T	GRD	-15V	-15V
5	A	OUT	OUT	OUT	IN	-15V	-15V	GRD	R/T	GRD	GRD	-15V
6	A	IN	OUT	OUT	IN	-15V	-15V	GRD	GRD	GRD	GRD	-15V
7	A	OUT	IN	OUT	IN	-15V	T/R	GRD	R/T	GRD	GRD	-15V
8	A	OUT	OUT	IN	IN	T/R	-15V	GRD	R/T	GRD	-15V	GRD
9	DUAL	OUT	OUT	OUT	OUT	-15V	R/T	R/T	R/T	GRD	-15V	-15V
10	DUAL	IN	OUT	OUT	OUT	-15V	R/T	R/T	R/T	R/T	-15V	-15V
11	DUAL	OUT	IN	OUT	OUT	-15V	GRD	GRD	R/T	R/T	-15V	-15V
12	DUAL	OUT	OUT	IN	OUT	T/R	R/T	R/T	R/T	GRD	-15V	-15V
13	DUAL	OUT	OUT	OUT	IN	-15V	R/T	GRD	R/T	GRD	GRD	-15V
14	DUAL	IN	OUT	OUT	IN	-15V	R/T	GRD	GRD	GRD	GRD	-15V
15	DUAL	OUT	IN	OUT	IN	-15V	GRD	GRD	R/T	GRD	GRD	-15V
16	DUAL	OUT	OUT	IN	IN	T/R	R/T	GRD	R/T	GRD	-15V	GRD
17	B	OUT	OUT	OUT	OUT	-15V	R/T	R/T	-15V	T/R	-15V	-15V
18	B	IN	OUT	OUT	OUT	-15V	R/T	R/T	T/R	T/R	-15V	-15V
19	B	OUT	IN	OUT	OUT	-15V	GRD	GRD	-15V	-15V	-15V	-15V
20	B	OUT	OUT	IN	OUT	T/R	R/T	R/T	-15V	T/R	-15V	-15V
21	B	OUT	OUT	OUT	IN	-15V	R/T	GRD	-15V	GRD	GRD	-15V
22	B	IN	OUT	OUT	IN	-15V	T/R	GRD	T/R	GRD	GRD	-15V
23	B	OUT	IN	OUT	IN	-15V	GRD	GRD	-15V	GRD	GRD	-15V
24	B	OUT	OUT	IN	IN	T/R	R/T	GRD	-15V	GRD	-15V	GRD

R/T = +0.3 VDC in RECEIVE and -13.5 VDC in TRANSMIT

T/R = +0.3 VDC in TRANSMIT and -13.5 VDC in RECEIVE

Table 3-1. VFO Biasing

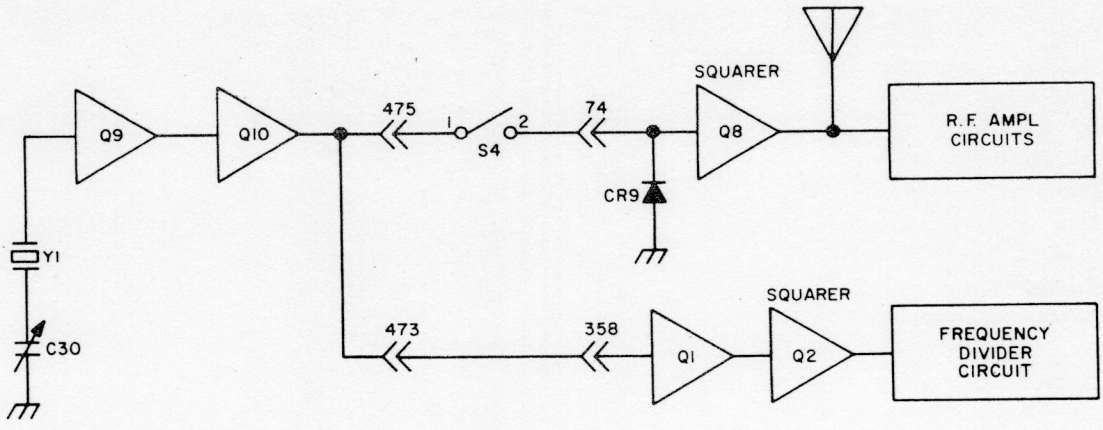


Figure 3-25. 100 kHz Oscillator Simplified Schematic Diagram

3.4.5 Actual Frequency Conversion

The previous paragraphs used approximate frequencies for explanation purposes. The exact oscillator and mixing frequencies to produce a USB transmit frequency of 7.2500 MHz is as follows:

43.1000	calibrator oscillator
- 8.8165	USB crystal oscillator
34.2835	IF board mixer IC output
- 3.3500	PTO module output
30.9335	IF board 30.1 to 31.1 mixer output
+ 8.8165	USB crystal oscillator
39.7500	IF board 39 to 40 mixer output
47.0000	Front End board local oscillator
-39.7500	IF board 39 to 40 mixer output
7.2500	Front End board mixer IC1 output (final transmit frequency in MHz)

3.5 100 kHz OSCILLATOR

The 100 kHz oscillator is located on the AGC Detector board. It is a continuous running master clock source for the frequency counter circuits. It also provides a 100 kHz frequency marker for receiver calibration purposes. A simplified block and signal path diagram for the 100 kHz oscillator is shown in Figure 3-25.

The 100 kHz oscillator is comprised of field effect transistor Q9 and 100 kHz crystal Y1. Capacitor C30 is adjusted to compensate for circuit tolerances permitting the oscillator frequency to be set to exactly 100,000 Hz. This is achieved by zero beating the 150th harmonic against WWV at 15 MHz. The output of transistor Q9 is routed through buffer amplifier transistor Q10 to AGC Detector board output pins 475 and 473. The RF signal level at each output pin is approximately 4 to 7 VPP. The 100 kHz signal from AGC Detector board output pin 475 is routed through the energized front panel "PULL TO CALIBRATE" switch S4 contacts 1 and 2 to the Front End board input pin 74. The 100 kHz signal is then shaped by the squaring amplifier comprised of diode CR9 and transistor Q8 in order to improve the harmonic output at 30 MHz. The output of transistor Q8 is applied to the receiver front end circuit.

The 100 kHz signal from AGC Detector board output pin 473 is routed to the Counter board input pin 358, and then routed through emitter follower transistor Q1 and level converter transistor Q2 to the input of the frequency divider circuits.

3.6 COUNTER

The basic concept of the frequency counter circuit employed by the Model CX7 is shown in Figure 3-26. To obtain a "RESET" and "READ" command signal, the master clock input signal is reduced in frequency by the clock divider chain. The "RESET" command signal instructs the RF counter chain when to start and when to stop processing the RF input countdown. The "READ" command signal instructs the input count gate when to pass and not to pass the RF input to the RF counter chain. The "READ" command also causes the read gate to turn-on or to turn-off the Nixie display tubes. The code converter circuit transposes the logic output of the RF counter chain into driving voltages that cause the appropriate numeral of each Nixie tube to illuminate.

The operating sequence of events for the frequency counter circuit is as follows:

a. The momentary reset pulse clears the RF counter chain outputs (causes the output states to return to the starting count of zero.)

b. The read command turns off the Nixie tubes for the duration of the read-in period and also enables the input count gate to pass the RF input to the RF counter.

c. The RF counter chain processes the RF input frequency countdown.

d. After a specific period of time, the read command switches to the read-out potential. The operation of the input count gate is inhibited. With no more inputs being applied to the RF counter chain, the last count produced by each divider circuit (in the RF counter chain) is retained. Their output states are, in-effect, a form of data storage.

e. When the read command switched to the read-out potential it also caused the read gate to turn-on the Nixie tubes. The converted output states of the RF counter chain is displayed for the duration of the read-out potential.

f. The reset pulse reoccurs causing a recycling of the events discussed in paragraph 3.6 a. through e.

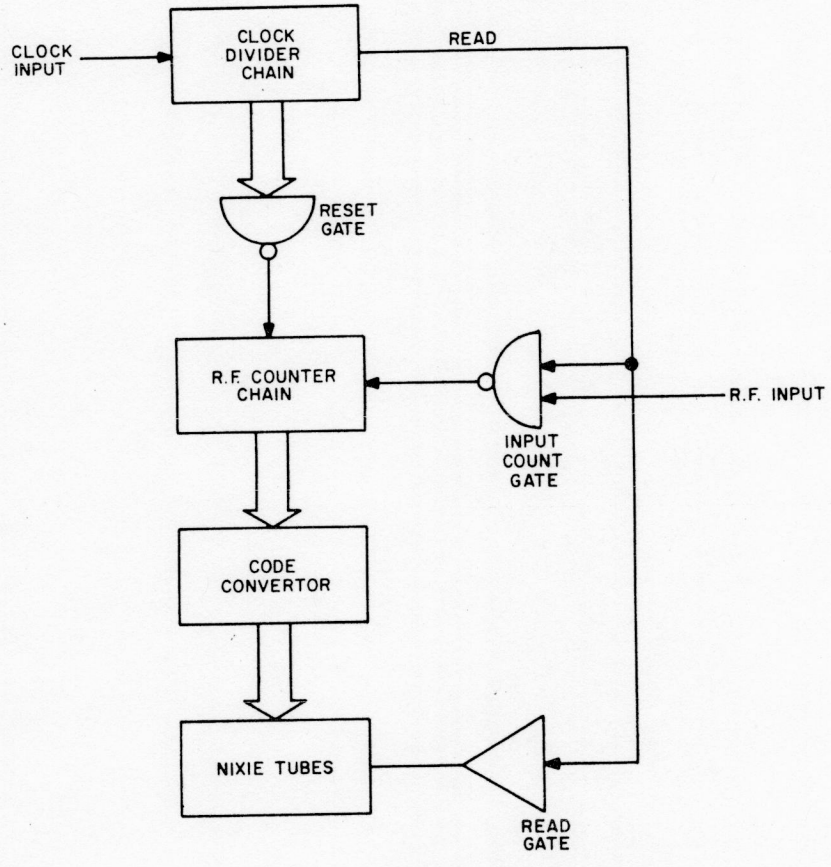


Figure 3-26. Simplified RF Counter Block Diagram

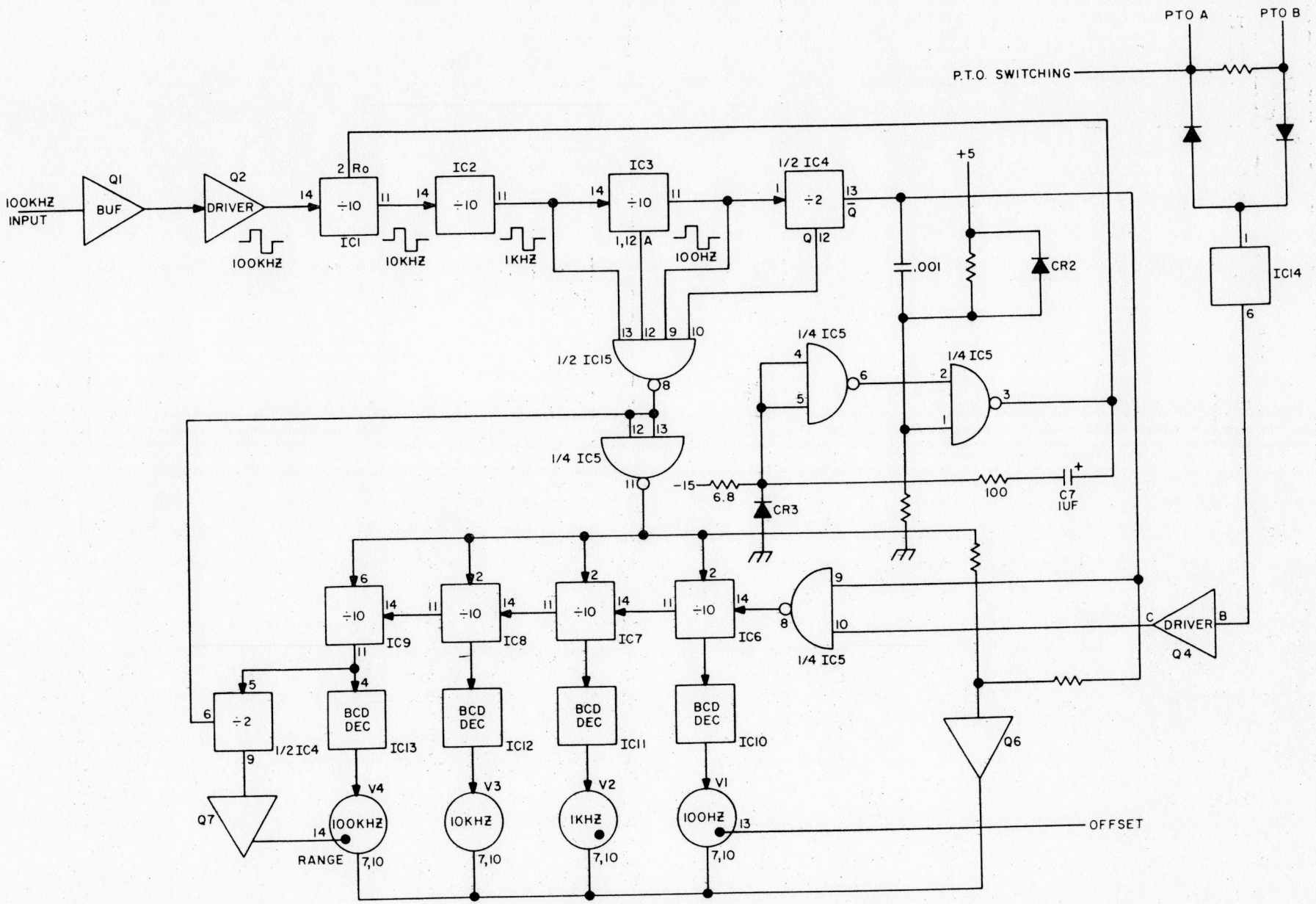


Figure 3-27. RF Counter Logic Block Diagram

Switch Position			PTO Switching Potential	PTO To Be Counted	
"B" (S2A)	"SPOT" (S2E)	RCV CHAN (S5)		In RCV	In XMIT
OUT	OUT	A	GRD	A	A
OUT	OUT	B	*T/R	B	A
OUT	OUT	DUAL	GRD	A	A
IN	OUT	A	GRD	A	A
IN	OUT	B	*T/R	B	A
IN	OUT	DUAL	GRD	A	A
OUT	IN	N/A	GRD	A	A
IN	IN	N/A	-15V	B	B

*T/R = +0.3 VDC in Receive
-13.5 VDC in Transmit

Table 3-2. PTO Switching Potential

Voltage				Count Equivalent
"A" Pin 12	"B" Pin 9	"C" Pin 8	"D" Pin 11	
0 VDC	0 VDC	0 VDC	0 VDC	0
+5 VDC	0 VDC	0 VDC	0 VDC	1
0 VDC	+5 VDC	0 VDC	0 VDC	2
+5 VDC	+5 VDC	0 VDC	0 VDC	3
0 VDC	0 VDC	+5 VDC	0 VDC	4
+5 VDC	0 VDC	+5 VDC	0 VDC	5
0 VDC	+5 VDC	+5 VDC	0 VDC	6
+5 VDC	+5 VDC	+5 VDC	0 VDC	7
0 VDC	0 VDC	0 VDC	+5 VDC	8
+5 VDC	0 VDC	0 VDC	+5 VDC	9

Table 3-3. BCD Count

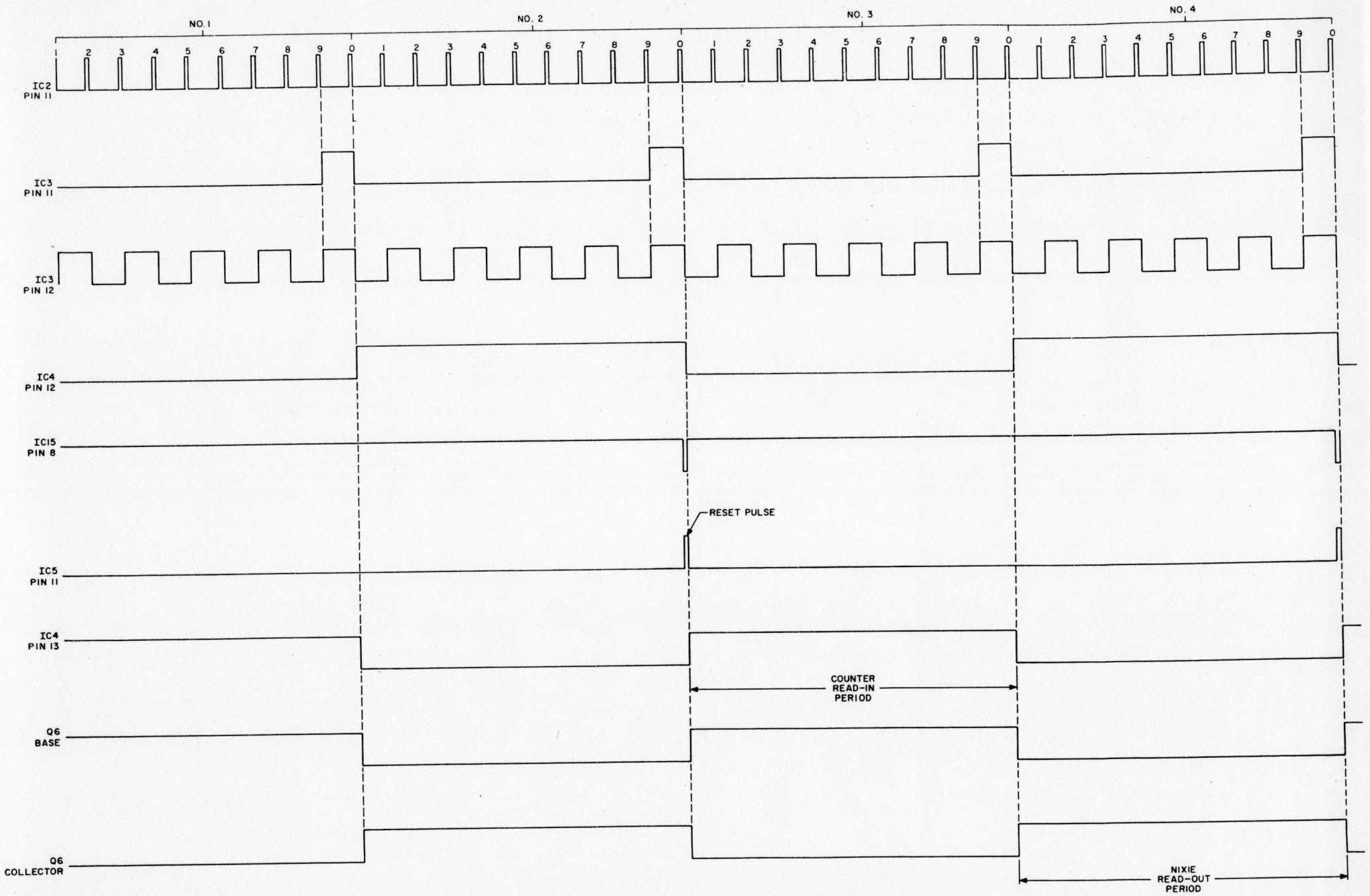


Figure 3-28. RF Counter Timing Block Diagram

The previous sequence of events occurs at a rate faster than the human eye can follow. Only the frequency display of the Nixie tubes is perceived.

A logic diagram of the actual Model CX7 frequency counter circuit is shown in Figure 3-27. The timing diagram shown in Figure 3-28 depicts the sequence of output events of the integrated circuits from which the reset, read-in, and read-out commands are derived.

The frequency from the 100 kHz standard on the AGC Detector board is routed through buffer transistor Q1 and driver transistor Q2. Transistor Q2 converts the transistor signal voltage level to integrated circuit voltage level. Integrated circuit IC1 divides the 100 kHz by a factor of ten. Integrated circuits IC2 and IC3 also function as divided by ten circuits producing outputs of 1 kHz and 100 Hz respectively. Integrated circuit IC4 divides the 100 kHz by a factor of two. The $\overline{Q}$ output of integrated circuit IC4 pin 13 provides the "READ" command signal to integrated circuit IC5 pin 9 and transistor Q6. The "READ" command consists of two potentials, which are, +3 to +5 VDC and a ground. The +3 to +5 VDC potential is referred to as the "READ-IN" command and the ground potential is referred to as the "READ-OUT" potential. When the read-in potential is applied to input count gate integrated circuit IC5 pin 9, any RF inputs that are applied to IC5 pin 10 will be inverted by IC5 and applied to integrated circuit IC6 pin 14. The read-in potential also forward biases transistor Q6, causing it to supply a ground that is used to lower the anode voltage of the Nixie tubes below the firing potential. Consequently, the Nixie tubes do not illuminate during the read-in potential. When the read-in potential switches to the read-out potential, the ground applied to integrated circuit IC5 pin 9 drives the output at IC5 pin 8 to a constant +5 VDC for the duration of the read-out potential (regardless of the potential of the RF input being applied to IC5 pin 10). During the read-out potential, transistor Q6 is reverse biased which permits the normal B+ potential to be applied to the Nixie tube anodes. Integrated circuit IC5 pin 3 is AC coupled to IC5 pins 4 and 5 permitting the two NAND gates to be utilized as a self-completing trigger circuit. The function of the trigger circuit is to provide a pulse that assists in ensuring the constant width of the reset pulse. The trigger pulse is a +3 to +5 VDC pulse occurring just prior to the read-in period and at all other times the IC5 pin 3 output is at ground potential. The reset pulse is originated when integrated circuit IC2 pin 11, IC3 pins 12 and 11 and IC4 pin 12 outputs are all within a +3 to +5 VDC potential which in turn causes the output of IC15 pin 8 to switch to a ground potential. The ground potential is inverted by integrated circuit IC5 to produce the actual reset pulse and is routed from IC5 pin 11 to each divide-by-ten circuit in the RF counter chain. The noninverted (ground) potential is used to clear the overrange divide-by-two flip-flop integrated circuit IC4.

The RF output from pin 3 of each PTO module is routed directly to the Counter board. PTO A is connected to Counter board input pin 354 and PTO B is connected to Counter board input pin 352. Each PTO RF output is applied to linear amplifier integrated circuit IC14 through the applicable steering diode CR5 or CR6. The diodes are biased so that only one PTO frequency can be applied to IC14 at any one time. The diode biasing a dependent upon the setting of the "TRANSMIT VFO-B" switch S2A, "SPOT" switch S2E and sometimes the "RECEIVE CHANNEL" switch S5A and S5B. The diode biasing (PTO switching potential) is either a ground, 0 VDC or -15 VDC. Table 3-2 lists which PTO switching potential is present for the different combinations of switch positions.

The PTO signal is amplified by integrated circuit IC14 and then applied to the base of waveshaper transistor Q4. The output of transistor Q4 is applied to integrated circuit IC5 input pin 10. The signal is permitted to pass through integrated circuit IC5 to integrated circuit IC6 input pin 14 whenever the positive read-in command is applied to integrated circuit IC5 input pin 9.

Each integrated circuit (IC6 through IC9) function as a divide-by-ten countdown divider. They function identically as the 50 Hz countdown chain except more of the outputs are used. For example, integrated circuit IC6 not only provides a divide-by-ten output to integrated circuit IC6 but also four outputs to integrated circuit IC10. The four outputs comprise what is referred to as a binary coded decimal (BCD) output. The voltage potential of the four outputs is a combination of zero or +5 VDC levels that form a code representative of the count (0 through 9) taking place in integrated circuit IC6 at any specific time. The actual voltage code and count equivalent is listed in table 3-3.

Integrated circuits IC10 through IC13 each perform an identical function. They are referred to as BCD to decimal decoders and each provides a ground to the applicable digit (0 through 9) of the Nixie tube.

3.7 POWER SUPPLY

The DC operating voltages for the Model CX7 are generated by the power supply circuits comprised of the Power Supply printed circuit board and miscellaneous electrical parts mounted on the CX7 chassis. A block diagram of the power supply circuit is shown in Figure 3-29.

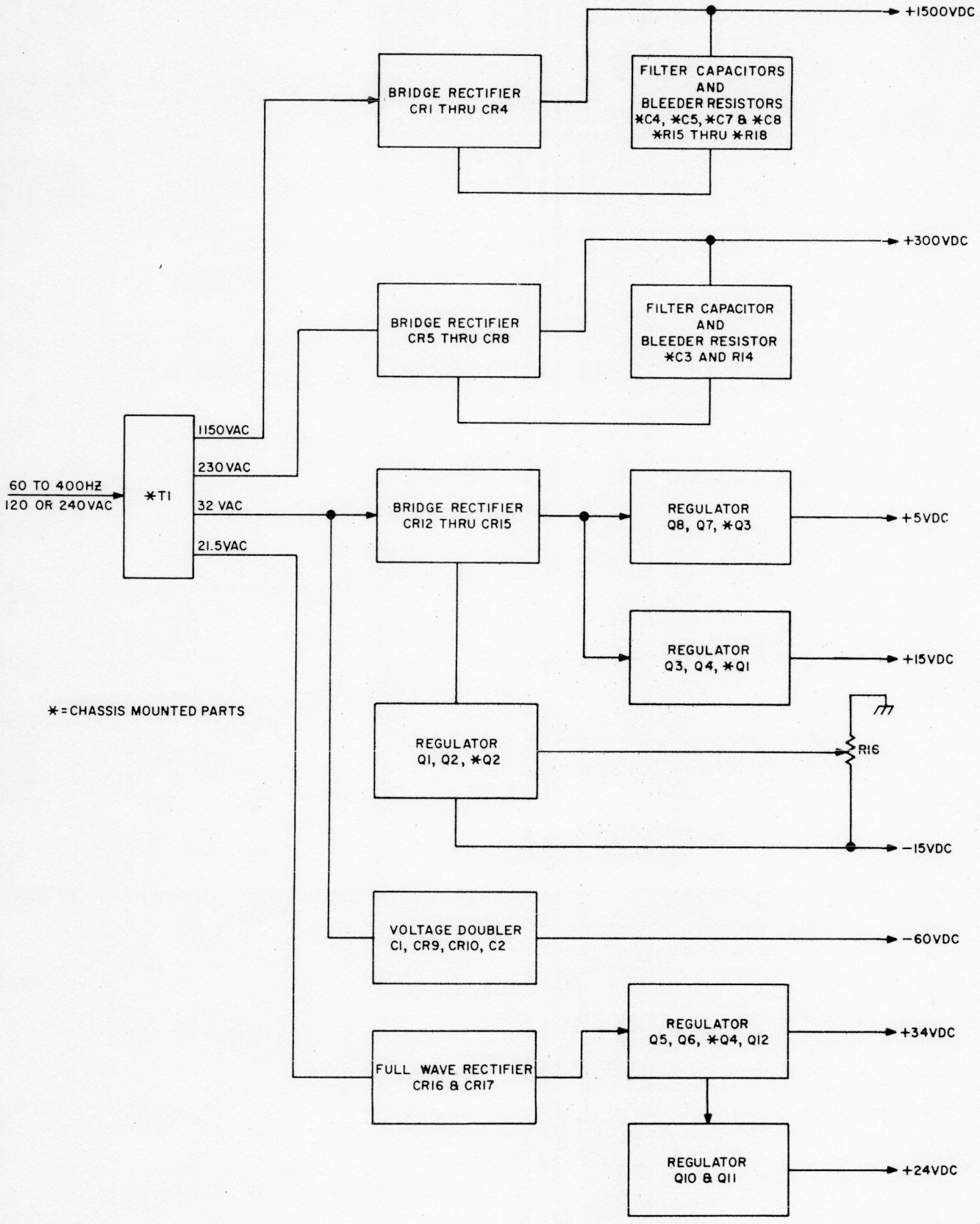


Figure 3-29. Power Supply Block Diagram

Primary power in the frequency range of 50 to 400 Hertz is routed from rear panel connector J6 pins 7 and 4, through a 5-ampere slo-blow fuse F1, thermistor RT1 and the energized "AC" switch to the primary windings of transformer T1. Strapping options for 120 or 240 VAC primary input voltage are provided at Power Supply printed circuit board input pins 163, 164, 165, and 166. The two T1 primary windings 1 to 2 and 3 to 4 are connected in parallel for 120 VAC operation or are connected in series for 240 VAC operation.

+1500 VDC Supply

The secondary windings 5 to 6 and 7 to 8 of transformer T1 are connected in series to provide a 1150 VAC input for the bridge rectifier comprised of diodes CR1 through CR4. The rectified output is filtered by capacitors C4, C5, C7, and C8. The output of the +1500 VDC supply is utilized by the plate of the power amplifier tube. The return lead of the supply is isolated from ground by resistors R1 and R40 to facilitate current sensing for the "PLATE" meter function.

+300 VDC Supply

The secondary winding 9 to 10 of transformer T1 provides a 230 VAC input for the bridge rectifier comprised of diodes CR5 through CR8. The rectified output is filtered by capacitor C3. The +300 VDC output is utilized by the screen of the power amplifier tube and the plate of the Counter board Nixie tubes. The return lead of the supply is isolated from ground by resistor R6 to facilitate current sensing for the "SCREEN" meter function.

-60 VDC Supply

The secondary winding 17 to 18 of transformer T1 provides a 30 VAC input to the voltage doubler comprised of capacitors C1 and C2 and diodes CR9 and CR10. The -60 VDC output of the voltage doubler is utilized by the control grid of the power amplifier tube.

+15, -15, and +5 VDC Supply

A simplified schematic of the +15, -15 and +5 VDC supply is shown in Figure 3-30. The secondary windings 15 to 16 and 17 to 18 of transformer T1 each provide 30 VAC to the bridge rectifier comprised of diodes CR12 through CR15. The positive output of the bridge is filtered by capacitor C9 and routed to the +5 and +15 VDC series regulators. The negative output of the bridge is routed to the -15 VDC series regulator. The circuit configuration permits referencing all of series regulators to the -15 VDC supply. The output of -15 VDC supply is adjusted by the setting of variable resistor R16. Each series regulator operates in the same manner: Two transistors are connected in a Darlington configuration, for added current-carrying capacity, feeding back regulation information to a control driver transistor.

+34 and +24 VDC Supply

A simplified schematic of the +34 and +24 VDC supply is shown in Figure 3-31. The secondary winding 11 to 12 and 13 to 14 of transformer T1 each provide 37 VAC to the full wave rectifier comprised of diodes CR16 and CR17. The output of the full wave rectifier is filtered by capacitor C2 and routed to the +34 VDC series regulator. The +34 VDC regulator operates in a similar manner as the series regulator previously described, with the exception of transistor Q12. The +34 VDC regulated output at the emitter of transistor Q4 is routed through one ohm resistor R41 to the +34 VDC distribution point. If the +34 VDC regulated output shorts to ground, transistor Q12 becomes forward biased which in turn reverse biases transistor Q5, resulting in interruption of the +34 VDC output.

Darlington connected transistors Q10 and Q11 further regulate the +34 VDC to +24 VDC.

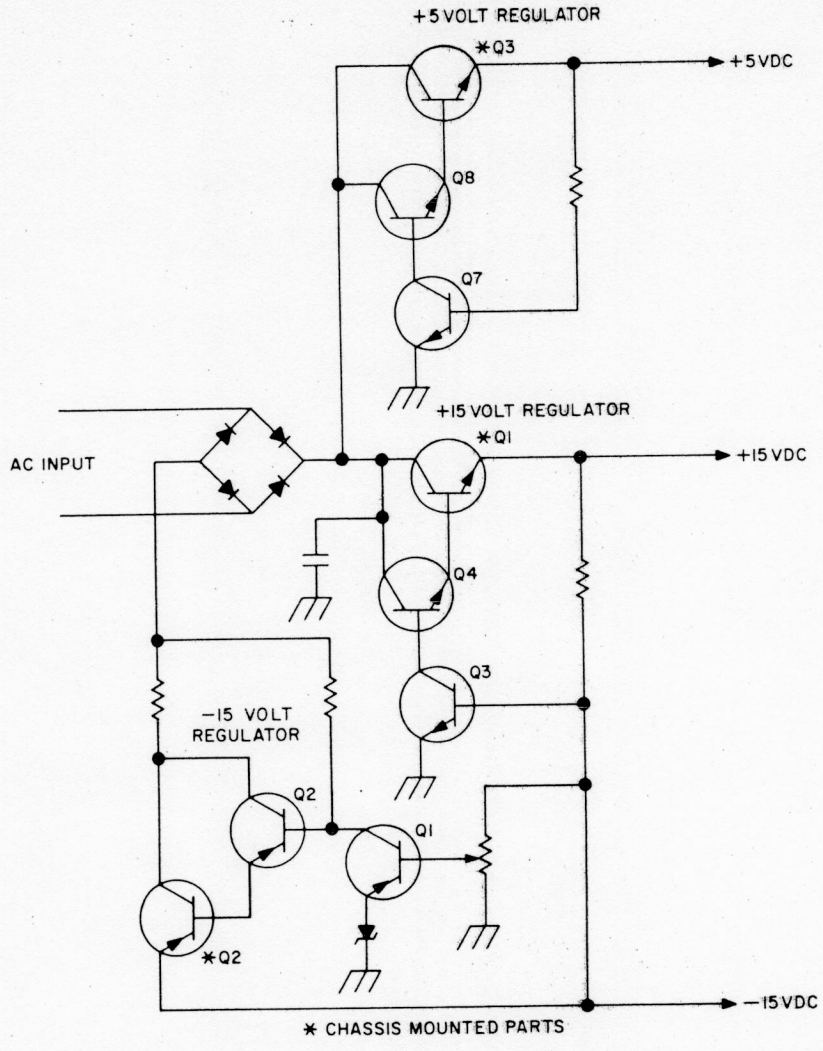


Figure 3-30. +15, -15 and +5 VDC Voltage Regulator Simplified Schematic Diagram

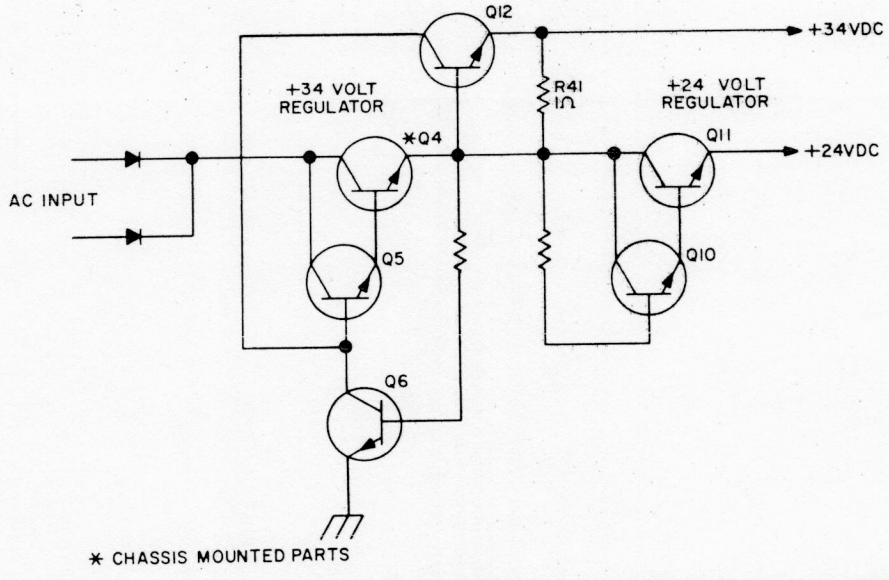


Figure 3-31. +34 and +24 VDC Voltage Regulator Simplified Schematic Diagram

SECTION IV

MAINTENANCE

4.1 INTRODUCTION

This section contains information for use in preventive or corrective maintenance, troubleshooting, component replacement and troubleshooting aids.

4.2 PREVENTIVE MAINTENANCE

4.2.1 General

Preventive maintenance consists of cleaning, visual inspection, lubrication, etc. Preventive maintenance performed on a regular basis may prevent breakdown and improve reliability. The Model CX7 should be cleaned as often as operating conditions require. Accumulation of dirt in the instrument can cause overheating and component breakdown. Dirt on components acts as an insulating blanket and prevents efficient heat dissipation. It also provides an electrical conduction path.

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Avoid chemicals which contain benzene, toluene, xylene, acetone, or similar solvents.

4.2.2 Cover Removal

Remove the seven Phillips-head screws located on the rear of the cover. Remove the two rear feet and the ten Phillips-head screws located on the bottom of the cover. From the rear, push the chassis slowly forward until the front panel protrudes from the cover about an inch. Grasp the front panel at the edges and carefully pull the chassis out of the cover.

4.2.3 Cleaning

a. Exterior. Loose dust accumulated on the outside of the Model CX7 can be removed with a soft cloth or small paint brush. The paint brush is particularly useful for dislodging dirt on and around the front panel controls. Dirt which remains can be removed with a soft cloth dampened in a mild detergent and water solution. Abrasive cleaners should not be used.

b. Interior. Dust in the interior of the transceiver should be removed occasionally due to its electrical conductivity under high humidity conditions. The best way to clean the interior is to blow off the accumulated dust with dry, low-velocity air. Remove any dirt which remains with a soft paint brush or a cloth dampened with alcohol of chlorothene-nu. A cotton-tipped applicator is useful for cleaning in narrow spaces and circuit boards.

The high voltage circuits, particularly parts located in the PA Assembly, should receive special attention. Excessive dirt in these areas may cause high-voltage arcing and result in improper operation.

4.2.4 Lubrication

a. Switches and Potentiometers. The reliability of potentiometers, rotary switches and other moving parts can be maintained if they are kept properly lubricated. Use a cleaning-type lubricant on switch contacts. Lubricate switch detents with a heavier grease. Potentiometers which are not permanently sealed should be lubricated with a lubricant which does not affect electrical characteristics. The pot lubricant can also be used on shaft bushings. Do not overlubricate.

4.2.5 Visual Inspection

The Model CX7 should be inspected occasionally for such defects as broken connections, damaged circuit boards, and heat-damaged parts.

The corrective procedure for most visible defects is obvious; however, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the transceiver; therefore, it is important that the cause of overheating be corrected to prevent recurrence of the damage.

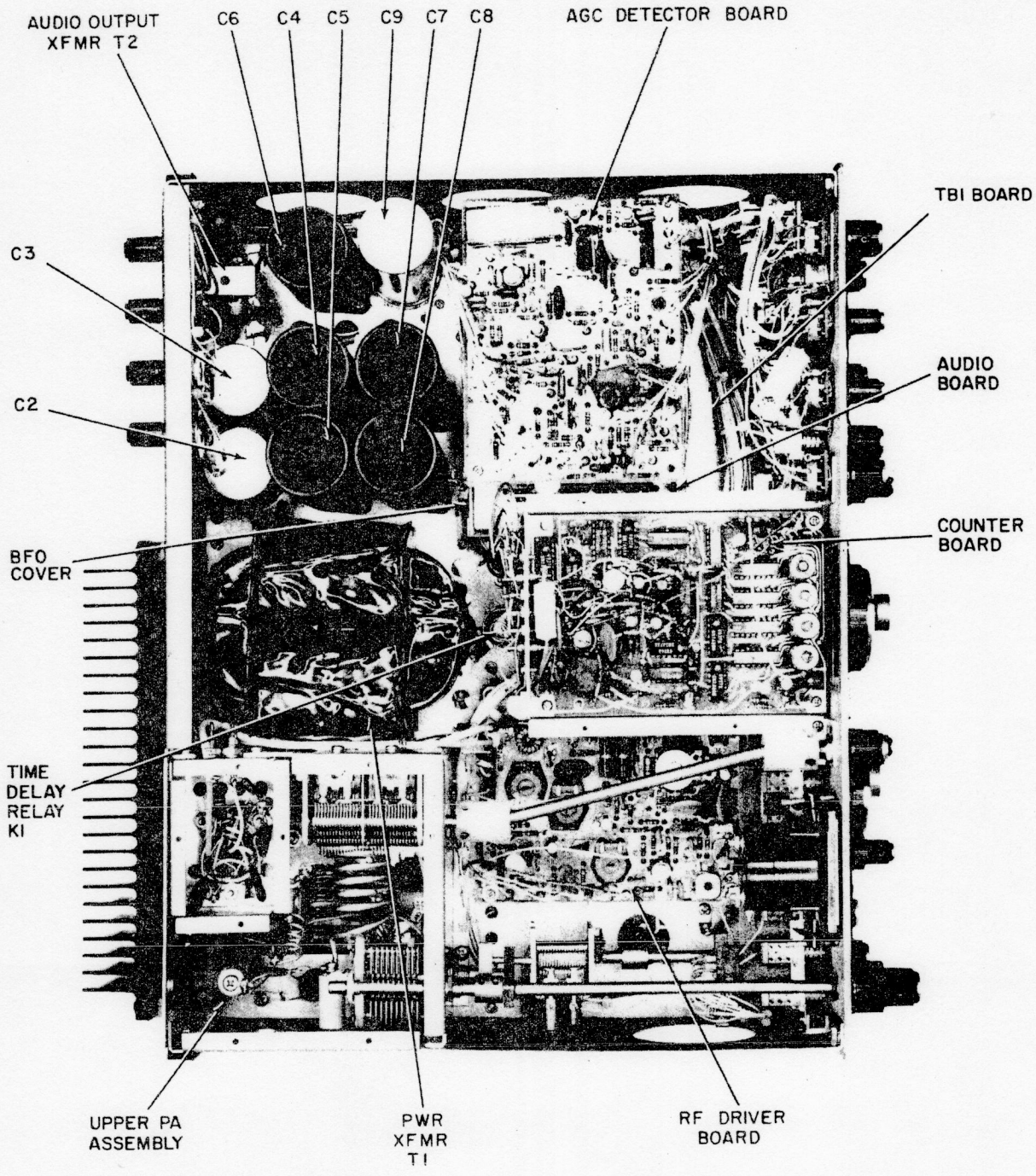


Figure 4-1. Model CX7 Top View (Sheet 1 of 2)

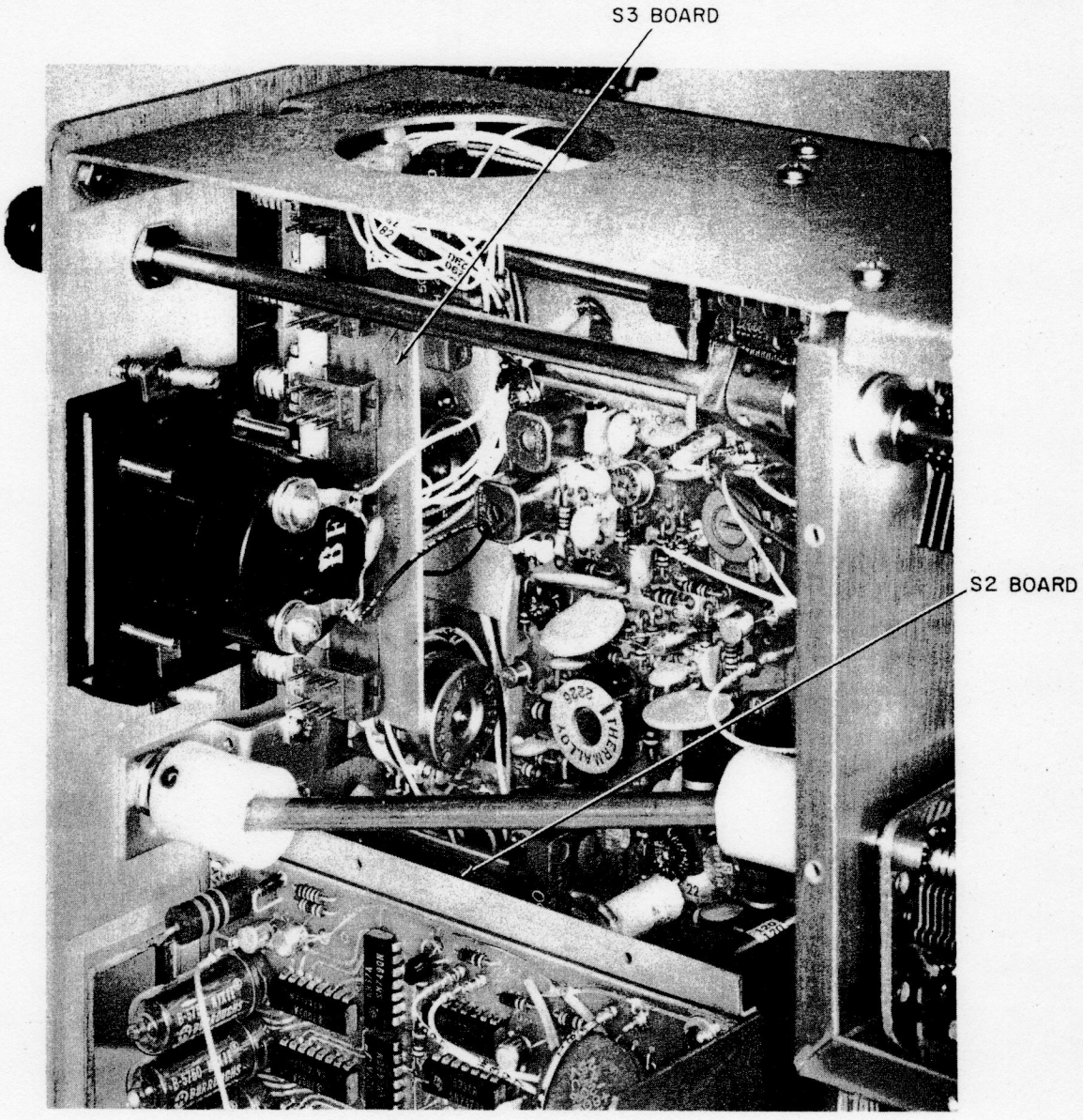


Figure 4-1. Model CX7 Top View (Sheet 2 of 2)

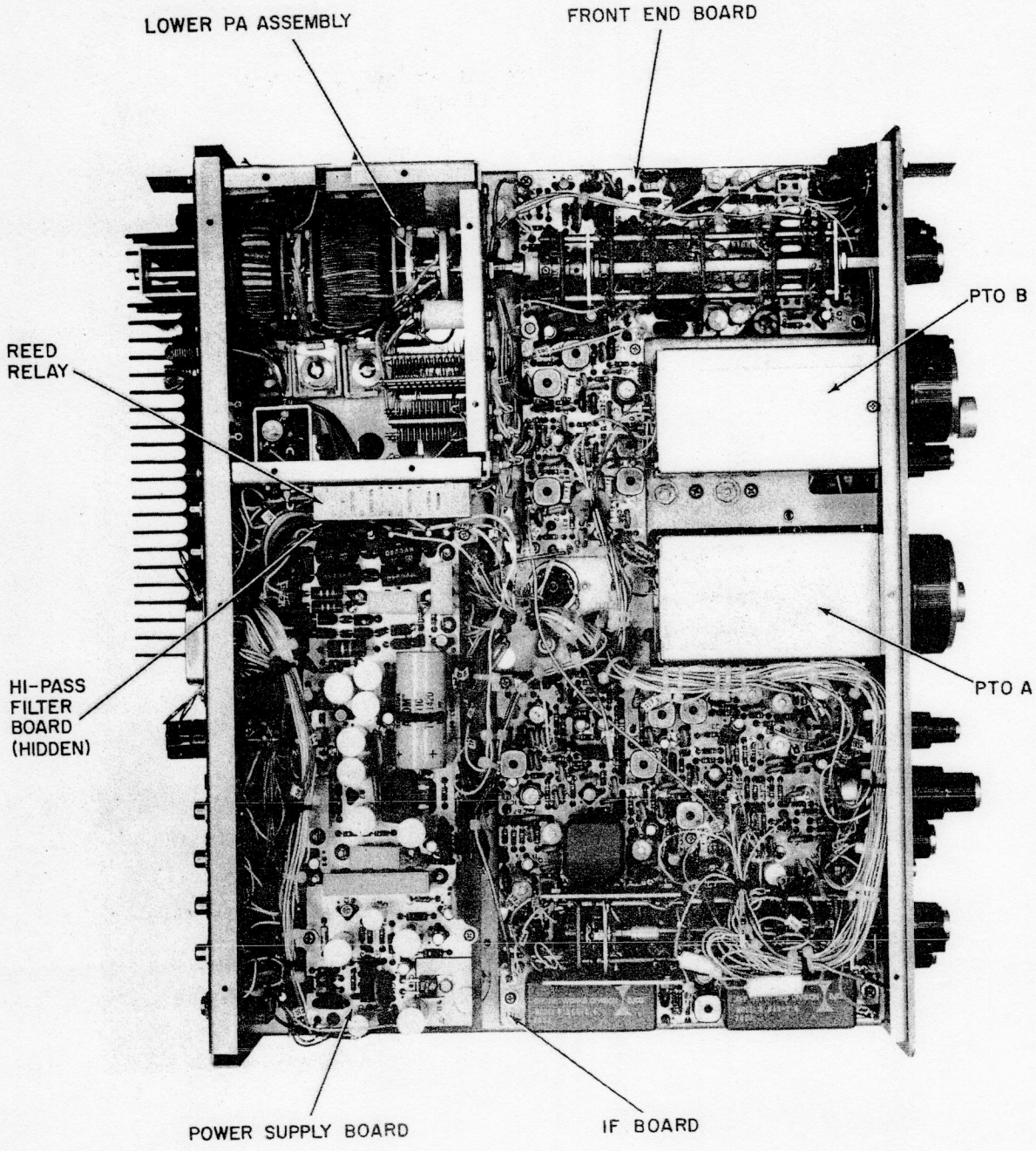


Figure 4-2. Model CX7 Bottom View

4.3 TROUBLESHOOTING

4.3.1 General

The information in the following paragraphs is provided to facilitate troubleshooting and should be used in conjunction along with other sections of this manual in locating a suspected defect.

4.3.2 Troubleshooting Techniques

This troubleshooting procedure is arranged in an order which checks the simple possibilities before proceeding with extensive troubleshooting. The first few checks assure proper operation and connection. If the trouble is not located by these checks, the remaining steps aid in locating the defective component. When the defective component is located, it should be replaced following the replacement procedures given under Corrective Maintenance.

a. Check Switch and Control Settings. Incorrect settings can indicate a trouble that does not exist. If there is any question about the correct function or operation of any control, see the Operating Instructions section of this manual.

b. Check Associated Equipment. Before proceeding with troubleshooting, check that the equipment used with this transceiver is operating correctly. Check that the interconnecting cables are not defective. Also, check the power source.

c. Isolate Trouble. Investigate the extent of the symptoms by monitoring the front panel meter and "KHZ" display while operating in different switch and control settings in various modes. Perform a visual check for damaged wires, electrical and mechanical parts, and printed circuit boards. Check for loose interconnections between printed circuit boards. First, isolate the trouble to a chassis mounted part or to the printed circuit board level and then to the circuit level using the checks given in paragraph 4.5.5. The type of pin connectors that are utilized provide a convenient means for printed circuit board isolation. For example, a short in the Power Supply board can be isolated by disconnecting the pin connectors, for that voltage, at the remaining boards.

d. Check Individual Parts. The following procedures describe methods of checking individual parts. Parts which are soldered in place are best checked by disconnecting one end. This isolates the measurement from the effects of surrounding circuitry.

1. Transistors and Integrated Circuits. The best check of operation is actual performance under operating conditions. If a part is suspected of being defective, it can best be checked by substituting a new part or one which has been checked previously. However, be sure that circuit conditions are not such that a replacement might also be damaged.

2. Diodes. A diode can be checked for an open or shorted condition by measuring the resistance between terminals. With an ohmmeter scale having an internal source of between 800 millivolts and 3 volts, the resistance should be very high in one direction and very low when the leads are reversed.

CAUTION

Do not use an ohmmeter scale that has a high internal current. High currents may damage the diode.

3. Resistors. Check the resistors with an ohmmeter. Check the Electrical Parts List for the tolerance of the resistors used in this instrument. Resistors normally do not need to be replaced unless the measured value varies widely from the specified value.

4. Inductors. Check for open inductors by checking continuity with an ohmmeter. Shorted or partially shorted inductors can usually be found by checking the waveform response when high-frequency signals are passed through the circuit. Partial shorting often reduces high frequency response (roll-off).

5. Capacitors. A leaky or shorted capacitor can best be detected by checking resistance with an ohmmeter on the highest scale. Do not exceed the voltage rating of the capacitor. The resistance reading should be high after initial charge of the capacitor. An open capacitor can best be detected with a capacitance meter or by checking whether the capacitor passes AC signals.

e. Repair and Readjust the Circuit. If any defective parts are located, follow the replacement procedures given in this section. Be sure to check the performance of any circuit that has been repaired or that has had any electrical parts replaced.

4.4 CORRECTIVE MAINTENANCE

4.4.1 General

Corrective maintenance consists of component replacement and Model CX7 repair. Special techniques required to replace components are given here.

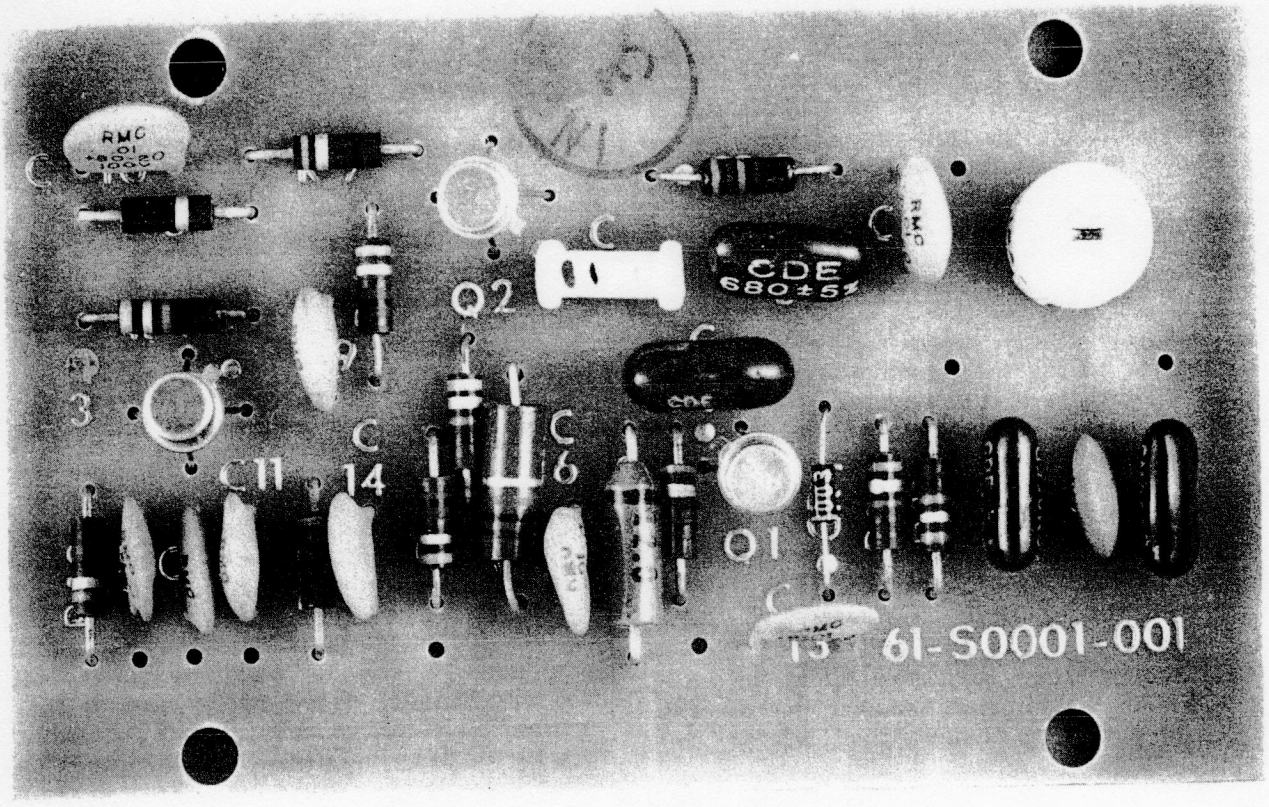
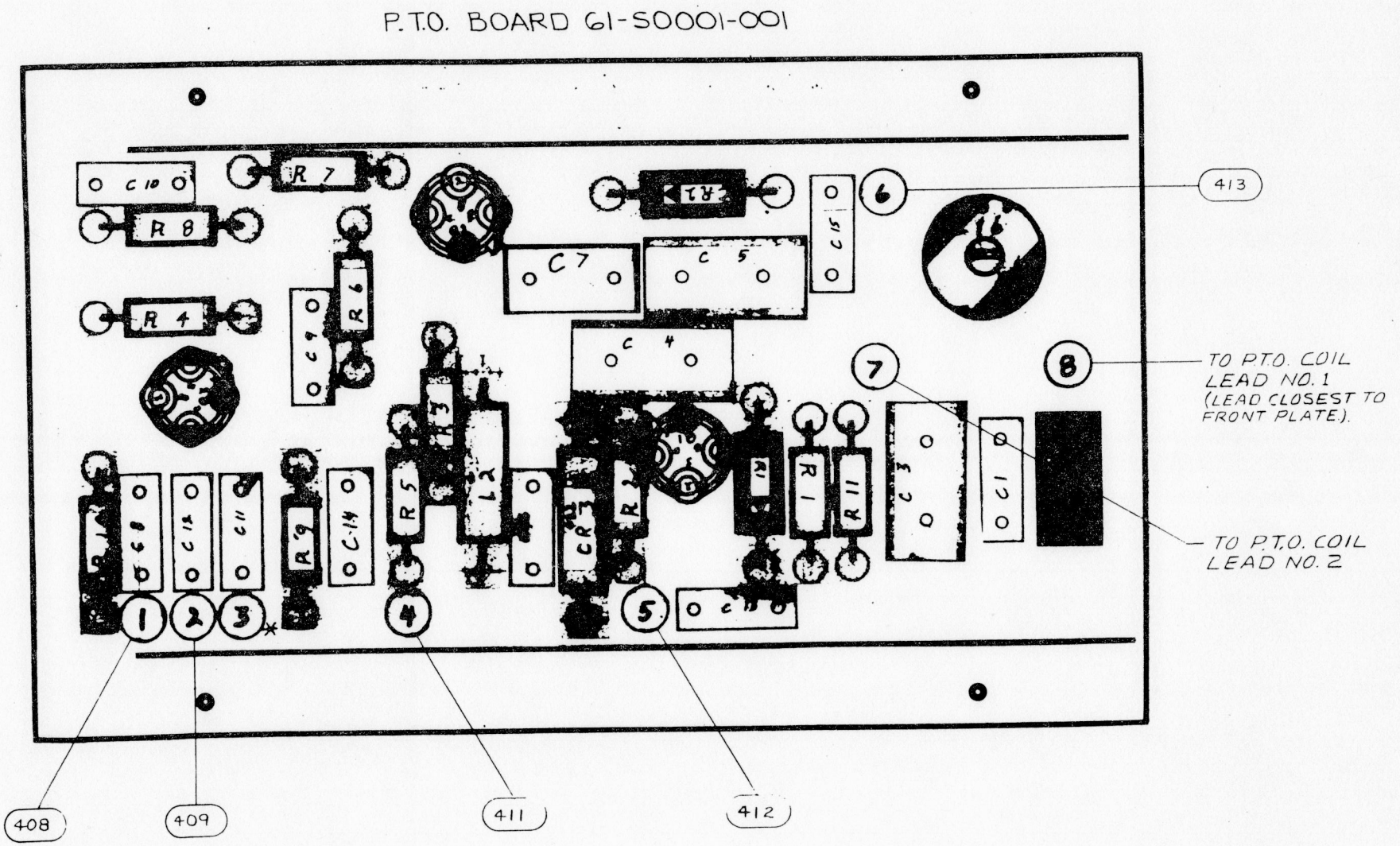


Figure 4-3. PTO Board (Sheet 1 of 2)

NOTES



NOTES:
1. * INDICATES DELETED ITEMS.
2. ○ INDICATES WIRE NUMBERS.

Figure 4-3. PTO Board (Sheet 2 of 2)

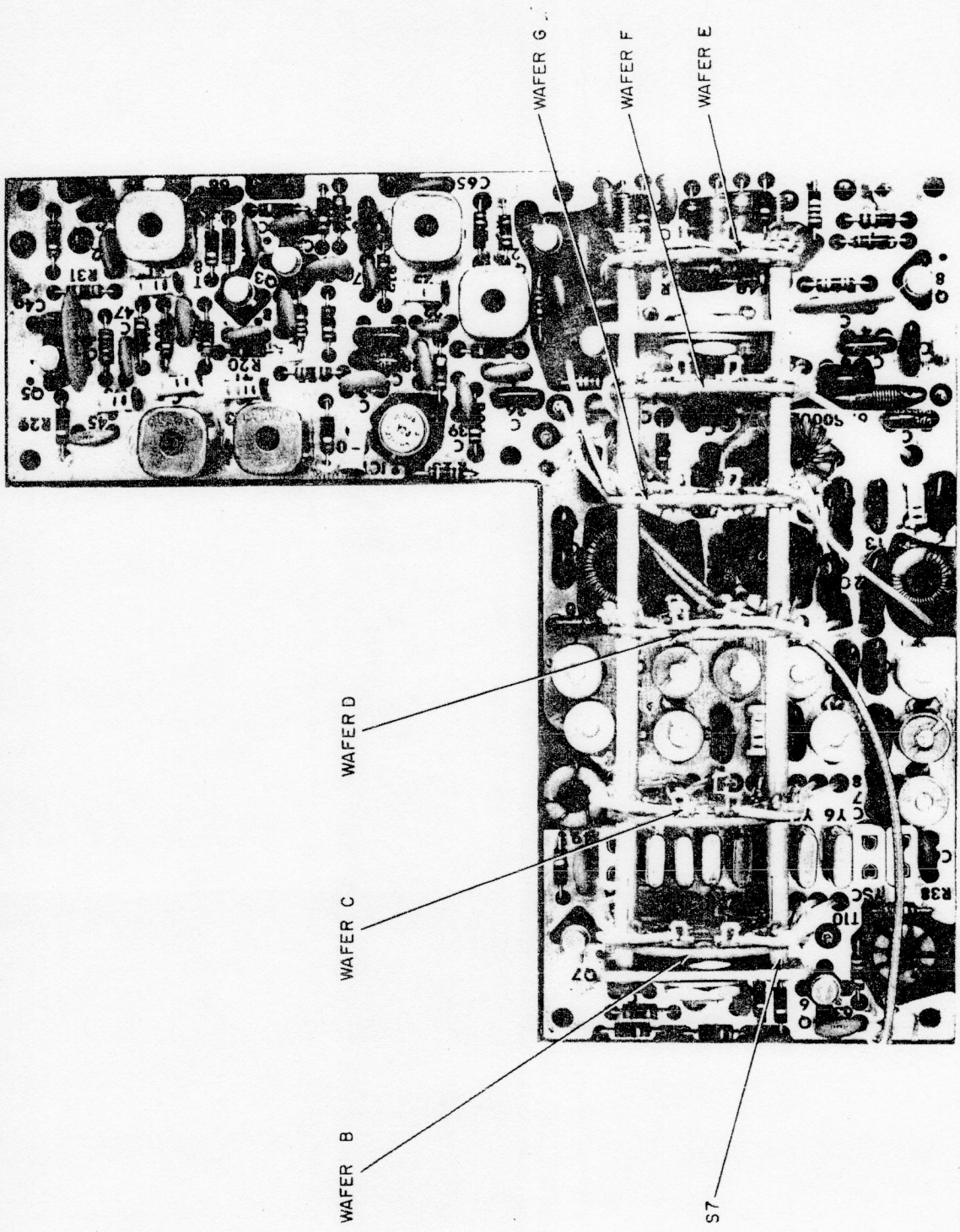
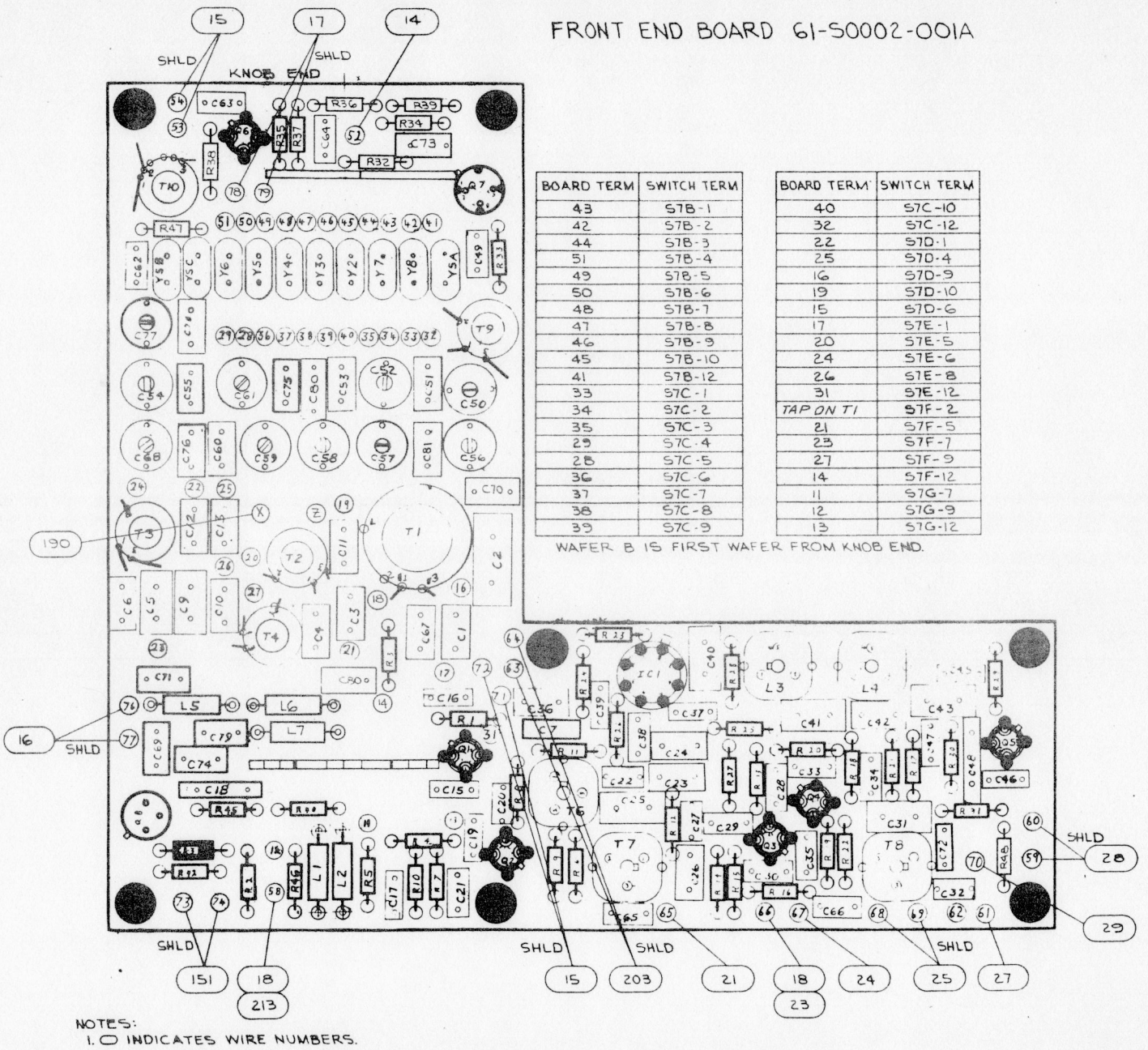


Figure 4-4. Front End Board (Sheet 1 of 2)



BOARD TERM	SWITCH TERM
43	S7B-1
42	S7B-2
44	S7B-3
51	S7B-4
49	S7B-5
50	S7B-6
48	S7B-7
47	S7B-8
46	S7B-9
45	S7B-10
41	S7B-12
33	S7C-1
34	S7C-2
35	S7C-3
29	S7C-4
28	S7C-5
36	S7C-6
37	S7C-7
38	S7C-8
39	S7C-9

BOARD TERM	SWITCH TERM
40	S7C-10
32	S7C-12
22	S7D-1
25	S7D-4
16	S7D-9
19	S7D-10
15	S7D-6
17	S7E-1
20	S7E-5
24	S7E-6
26	S7E-8
31	S7E-12
TAP ON T1	S7F-2
21	S7F-5
23	S7F-7
27	S7F-9
14	S7F-12
11	S7G-7
12	S7G-9
13	S7G-12

WAFER B IS FIRST WAFER FROM KNOB END.

Figure 4-4. Front End Board (Sheet 2 of 2)

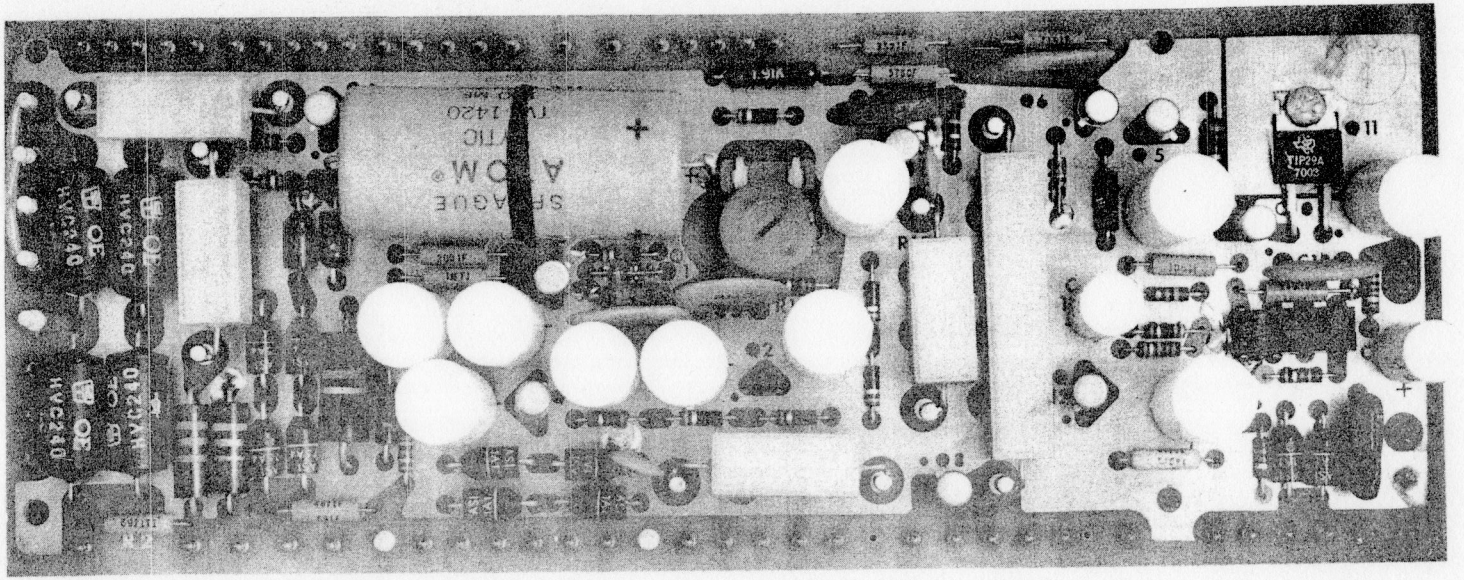


Figure 4-5. Power Supply Board (Sheet 1 of 2)

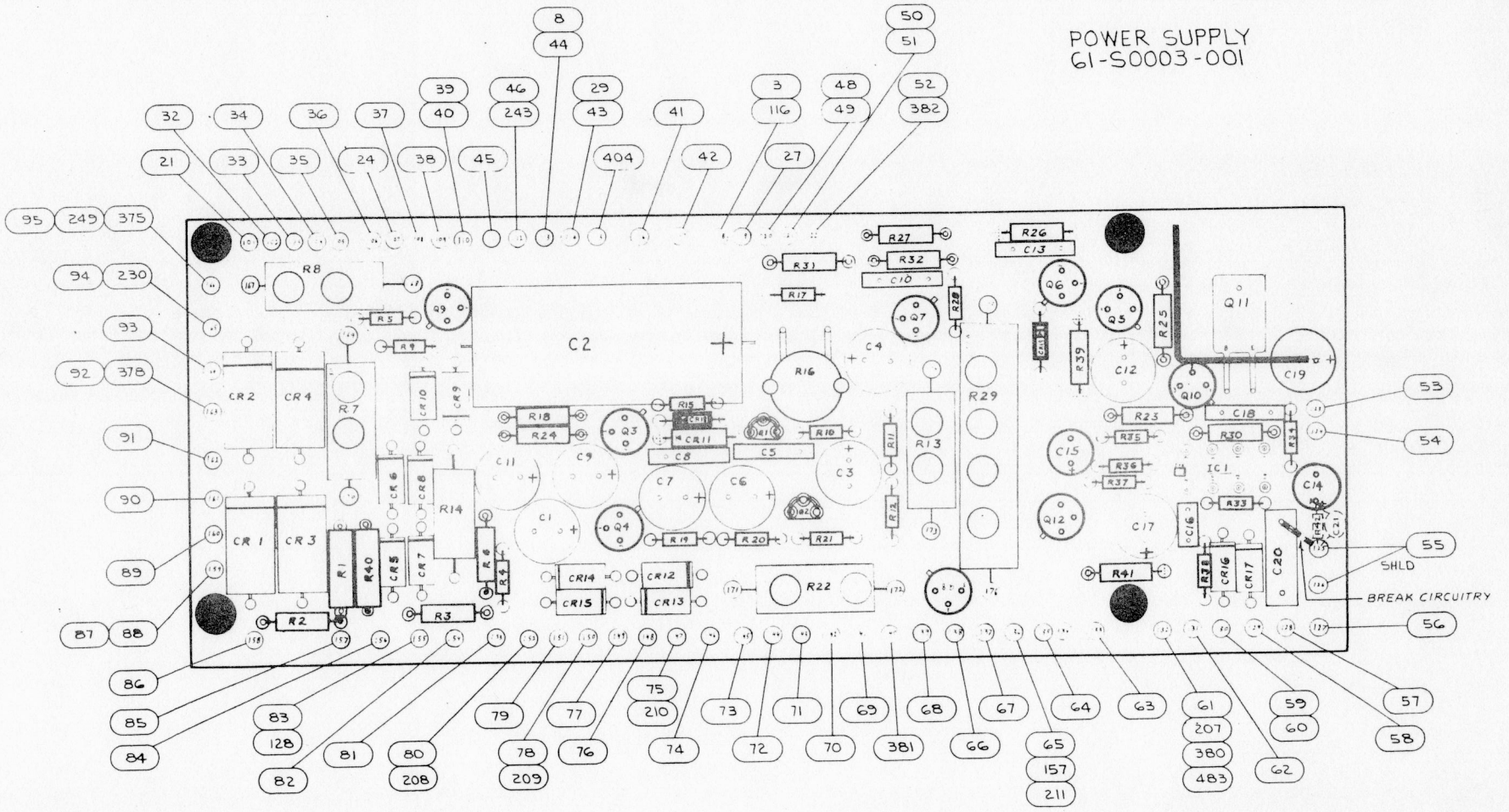


Figure 4-5. Power Supply Board (Sheet 2 of 2)

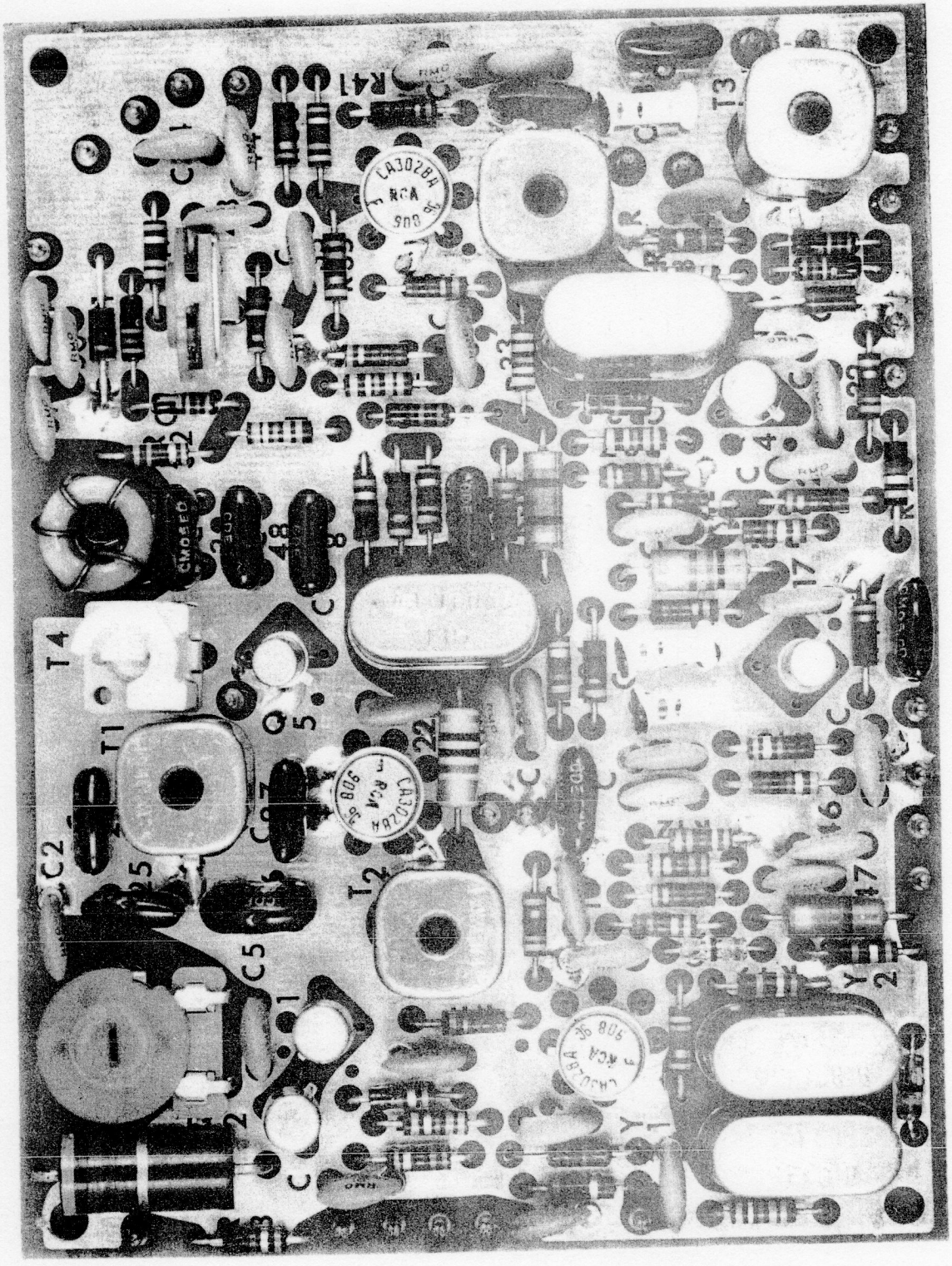
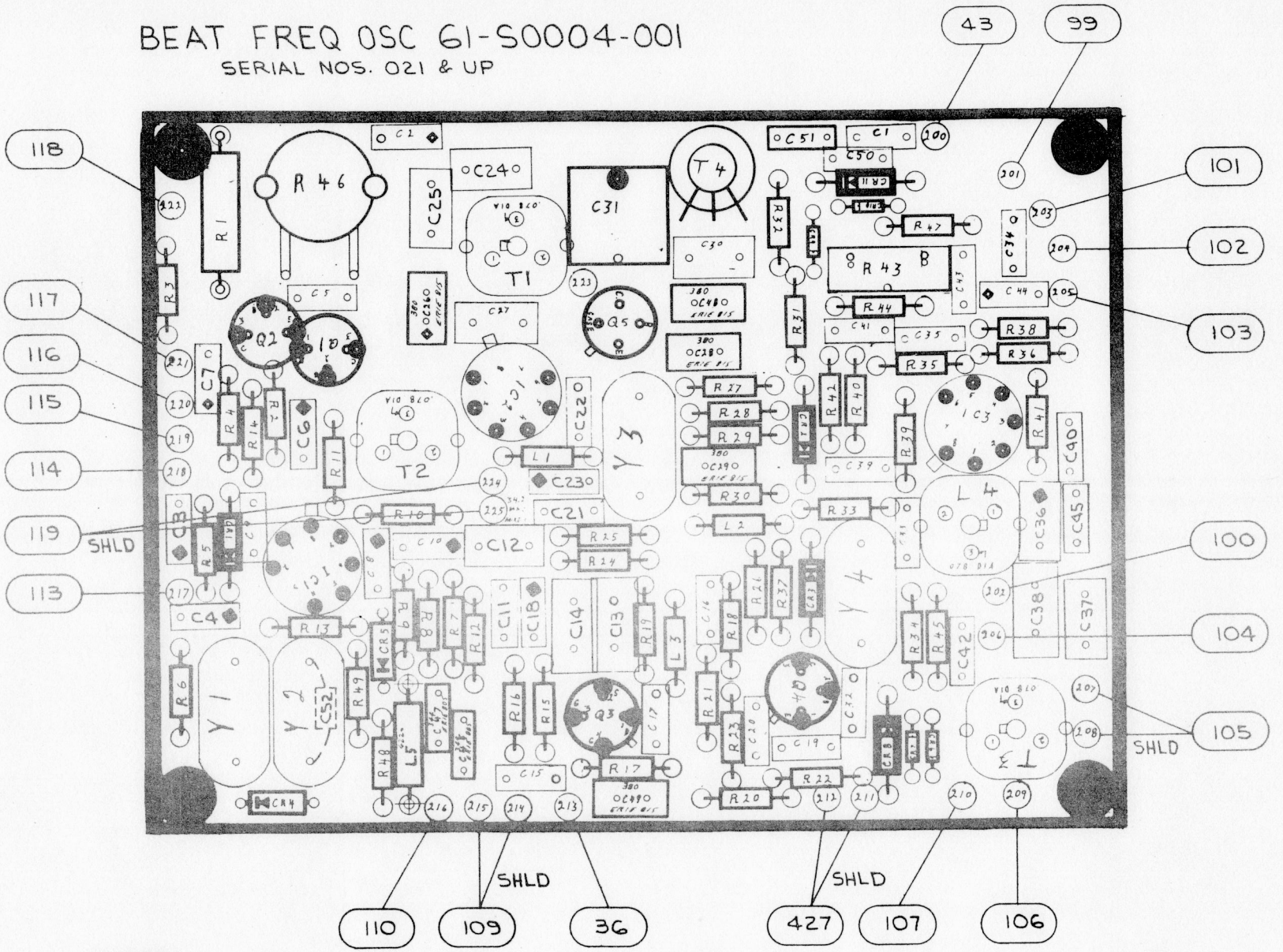


Figure 4-6. BFO Board (Sheet 1 of 2)



NOTES:
1. ○ INDICATES WIRE NUMBERS.
2. C52 MOUNTED ON CIRCUIT SIDE.

Figure 4-6. BFO Board (Sheet 2 of 2)

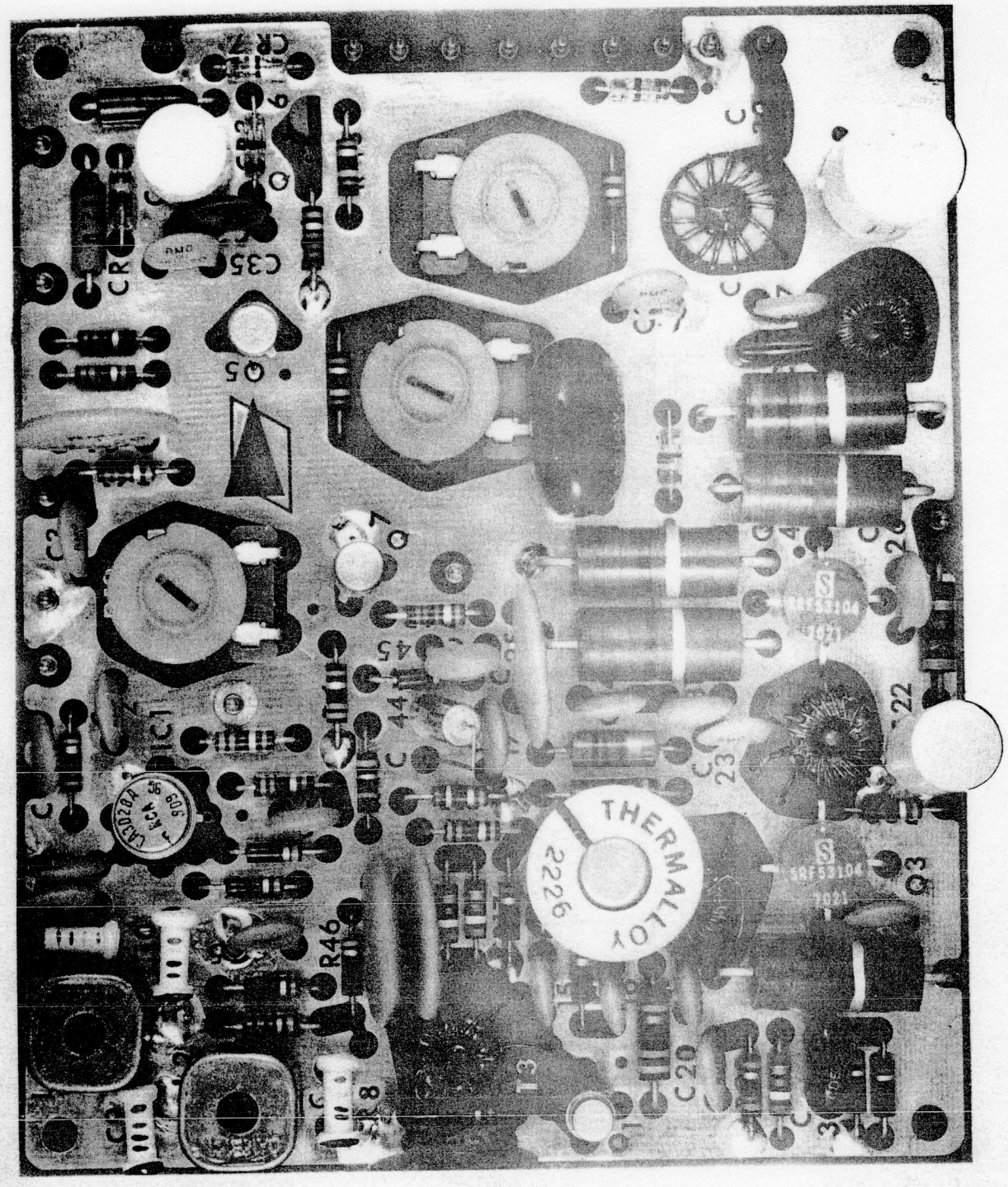


Figure 4-7. RF Driver Board (Sheet 1 of 2)

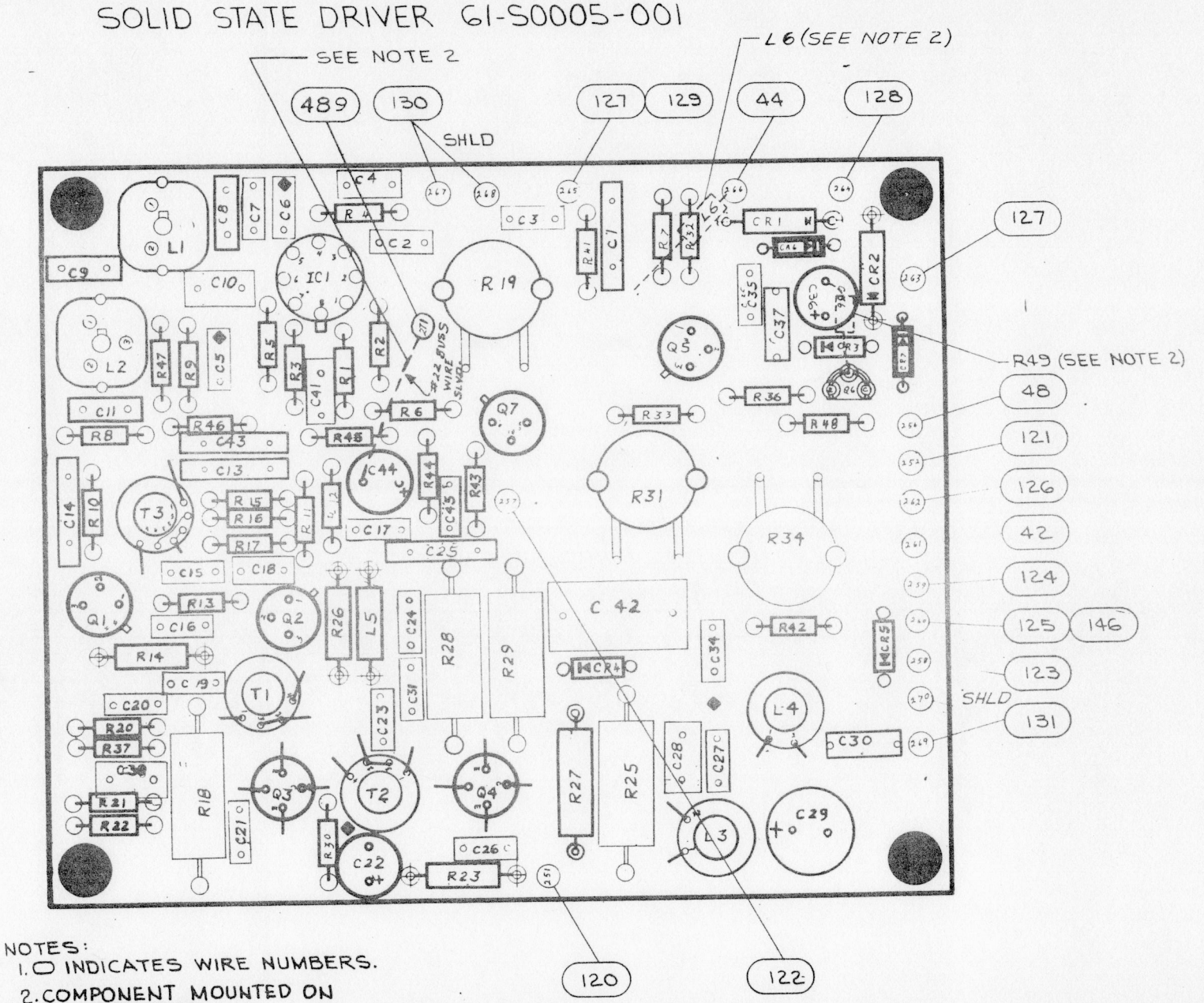
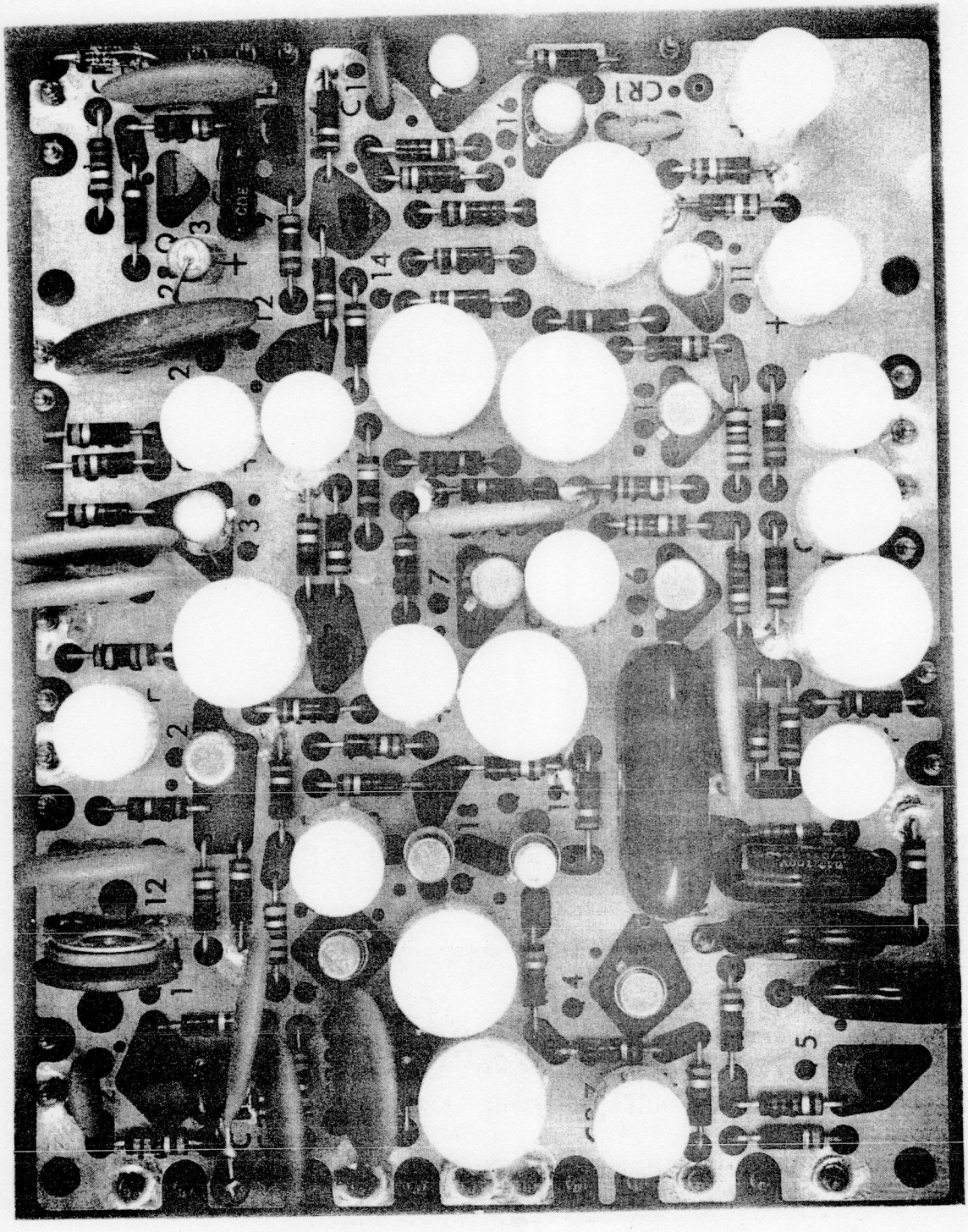


Figure 4-7. RF Driver Board (Sheet 2 of 2)


CR1
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
C19
C20
C21
C22
C23
C24
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
C37
C38
C39
C40

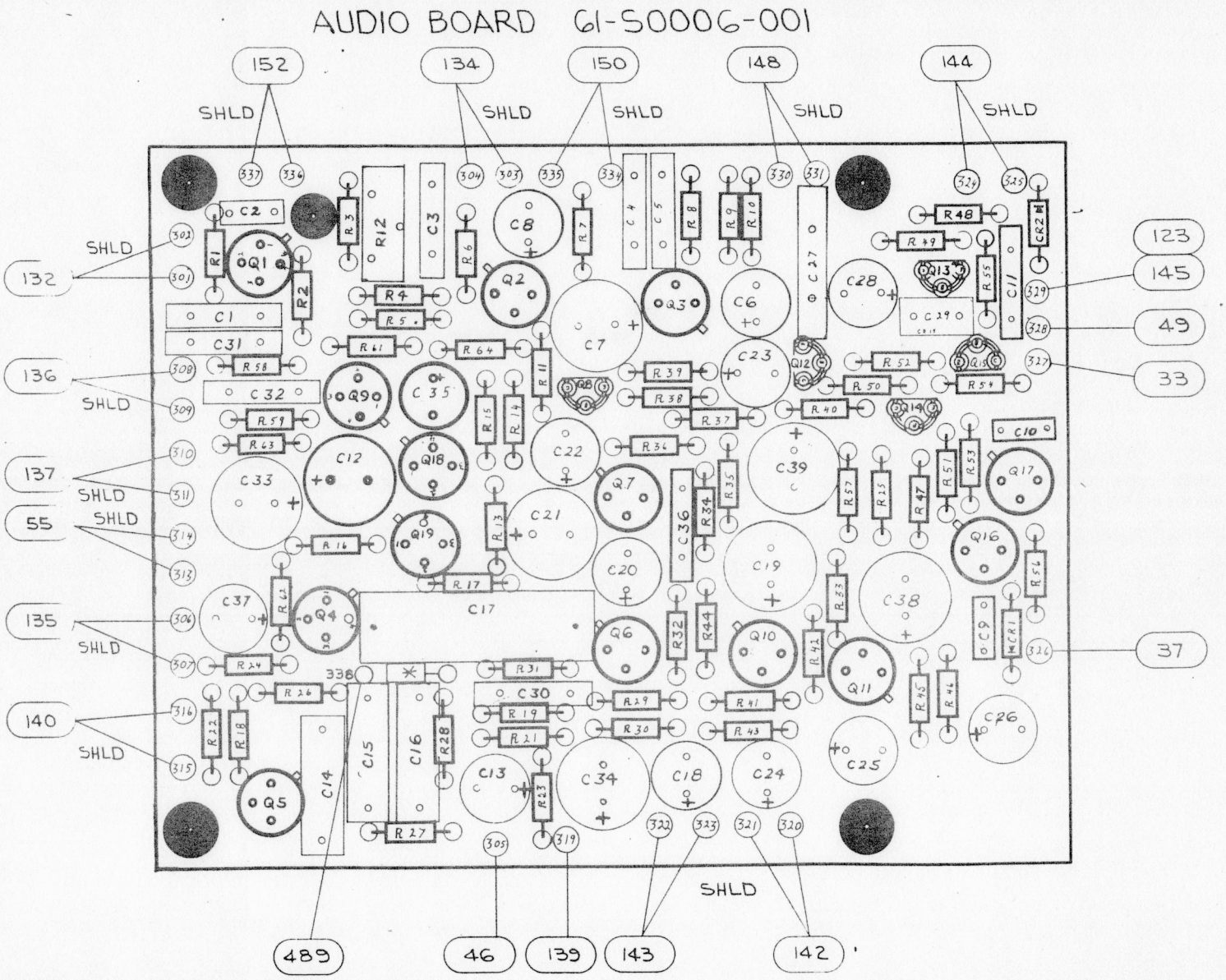


Figure 4-8. Audio Board (Sheet 2 of 2)

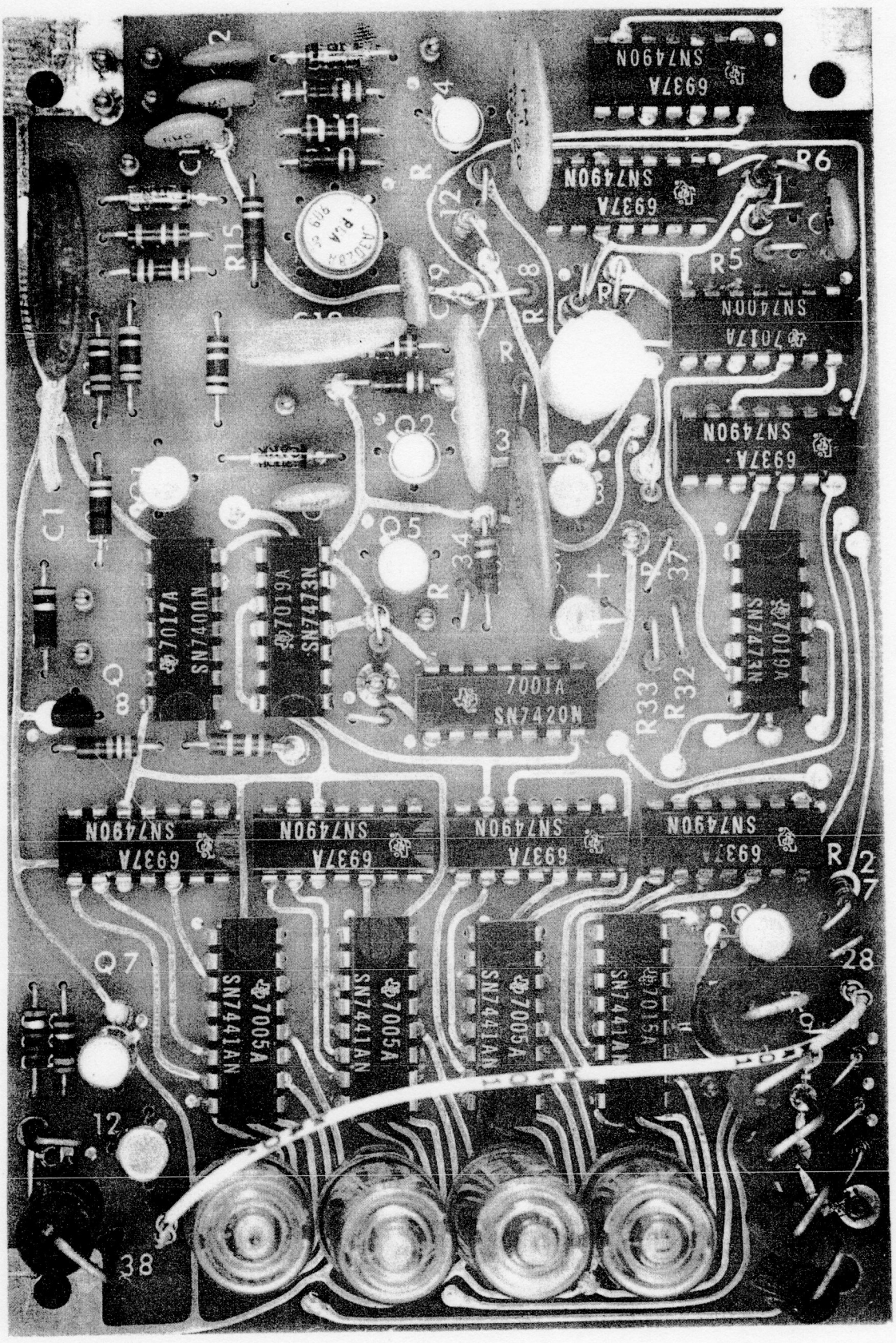


Figure 4-9. Counter Board (Sheet 1 of 2)

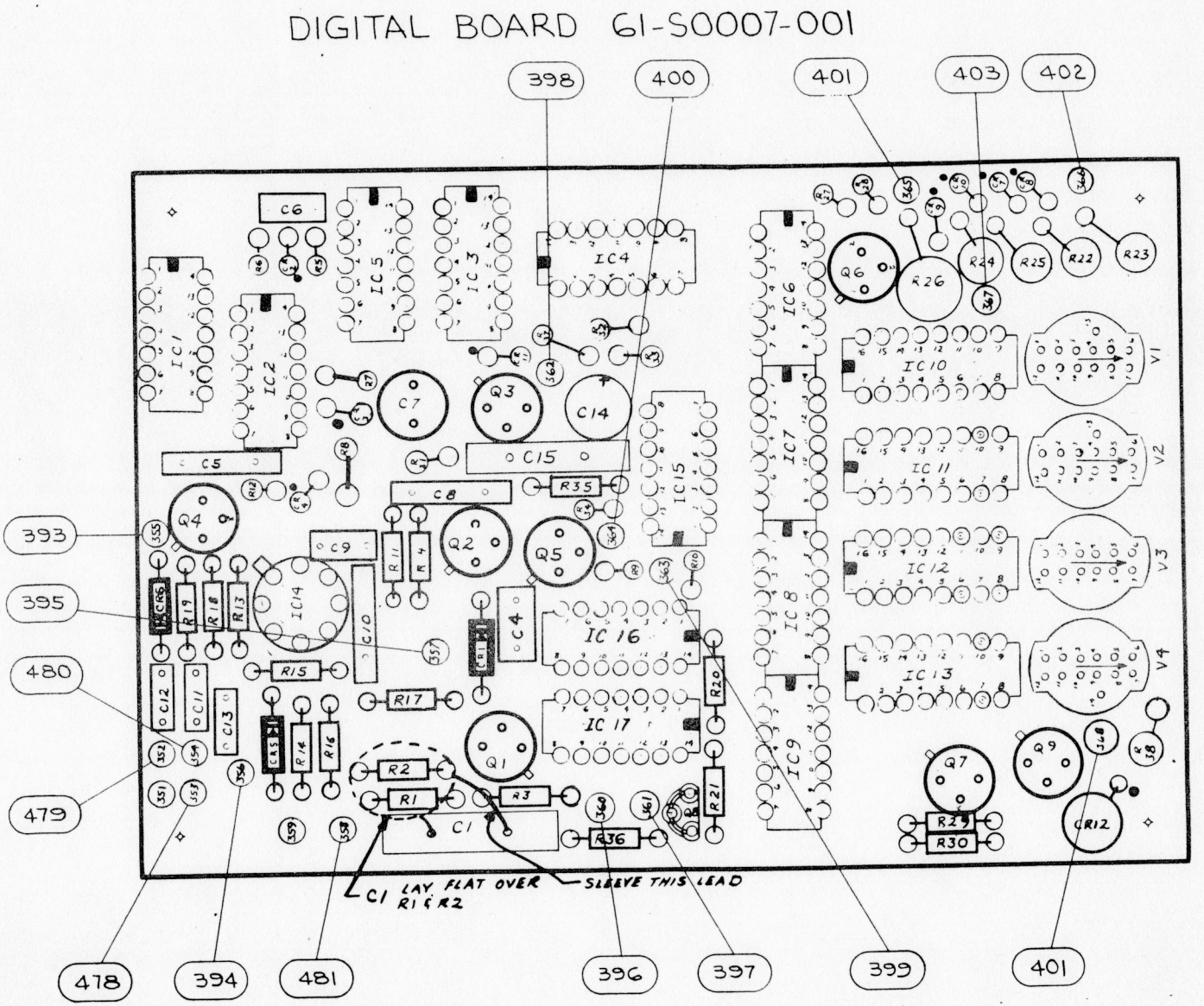


Figure 4-9. Counter Board (Sheet 2 of 2)

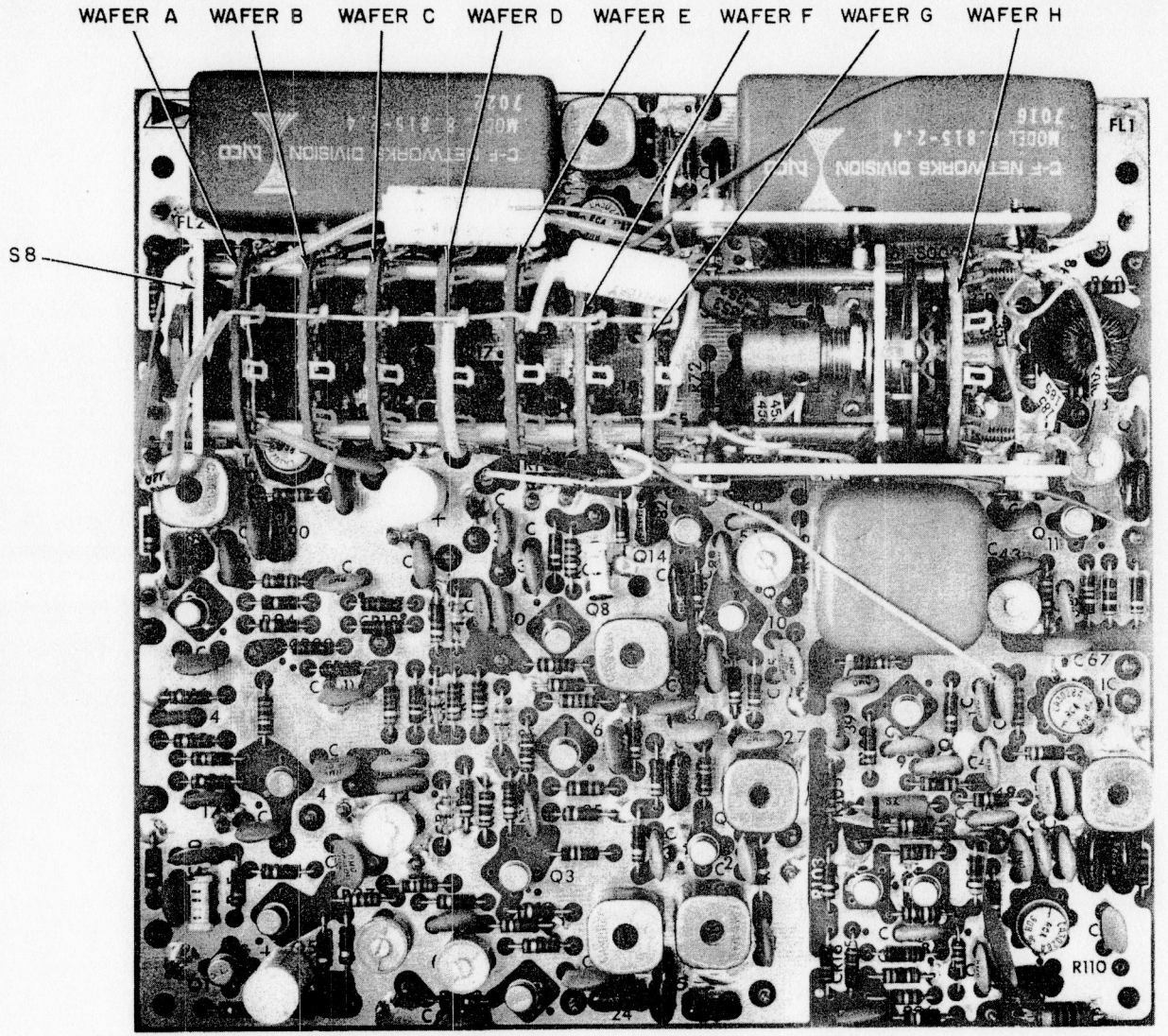


Figure 4-10. IF Board (Sheet 1 of 2)

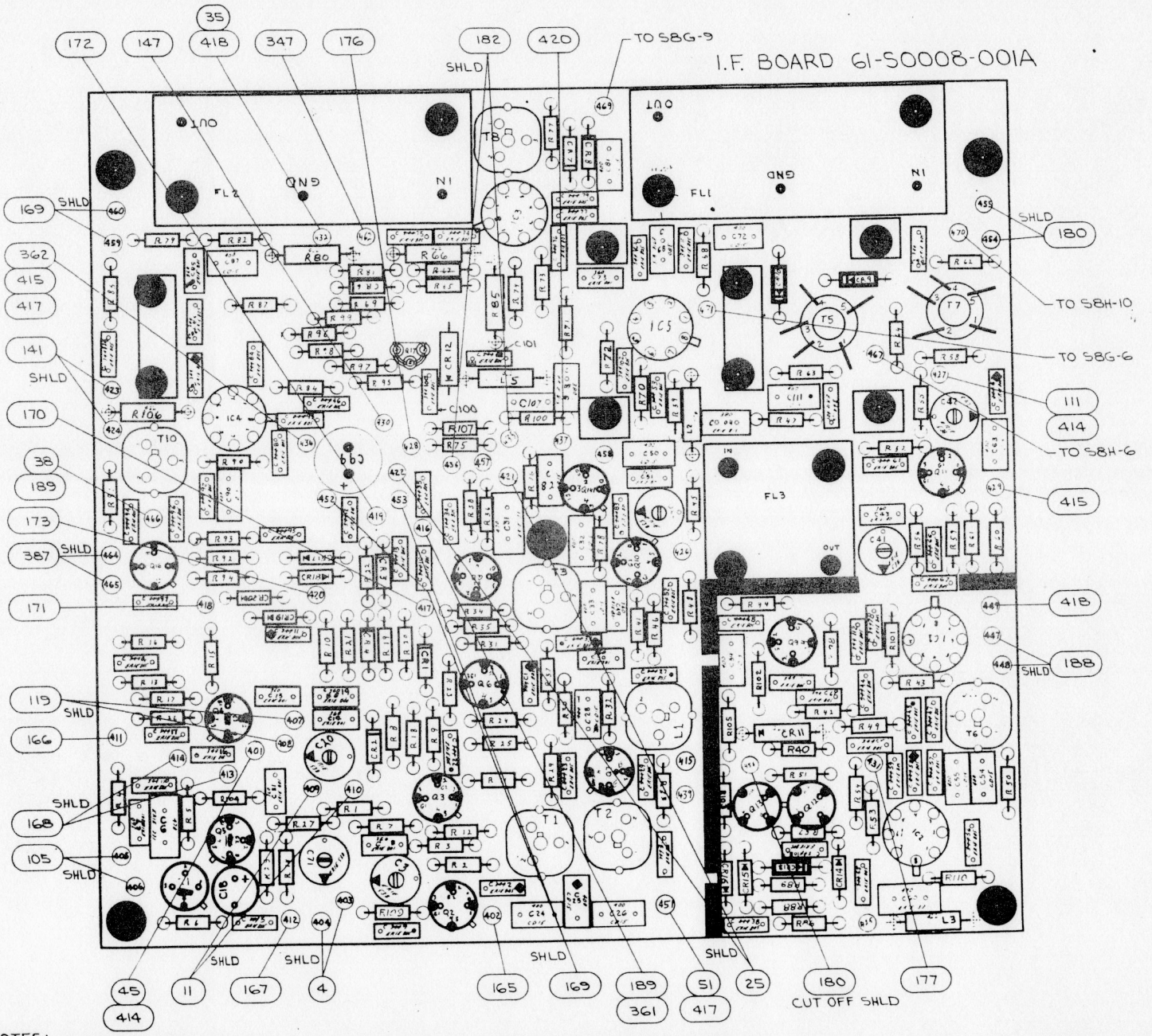


Figure 4-10. IF Board (Sheet 2 of 2)