BIPOLAR LINEAR INTEGRATED CIRCUIT
SILICON MONOLITHIC

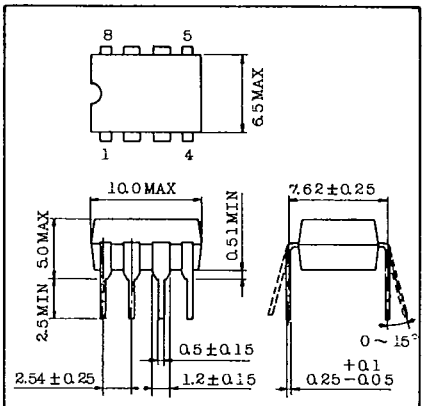
TA7504P/S

T-79-05-10

SINGLE OPERATIONAL AMPLIFIER
OPERATIONAL AMPLIFIER
DC AMPLIFIER

- High Gain : G_V=1×10^5 (Typ.)
- Low Power Dissipation : P_D=50mW (Typ.)
- High Common Mode Input Voltage : CMV_{IN}=±13V (Typ.)
- High Differential Input Voltage: DV_{IN}=30 (Typ.)
- Low Input Offset Voltage : V_{IO}=1mV (Typ.)
- No Frequency Compensation
- Absence of Latch-up
- Offset Null Capability
- Short Circuit Protection

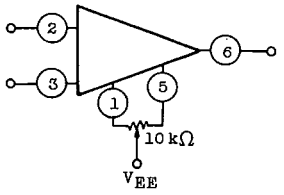
Unit in mm



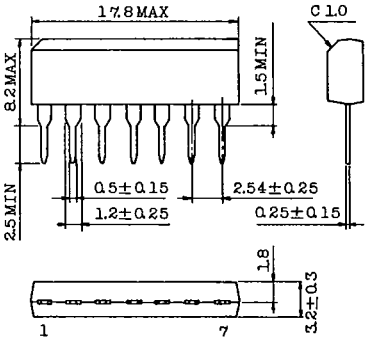
Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.8 leads.

JEDEC	—
TOSHIBA	3D8A-P

VOLTAGE OFFSET NULL CIRCUIT



Unit in mm



Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 lead.

JEDEC	—
TOSHIBA	S7A-P

MAXIMUM RATINGS (Ta=25°C)

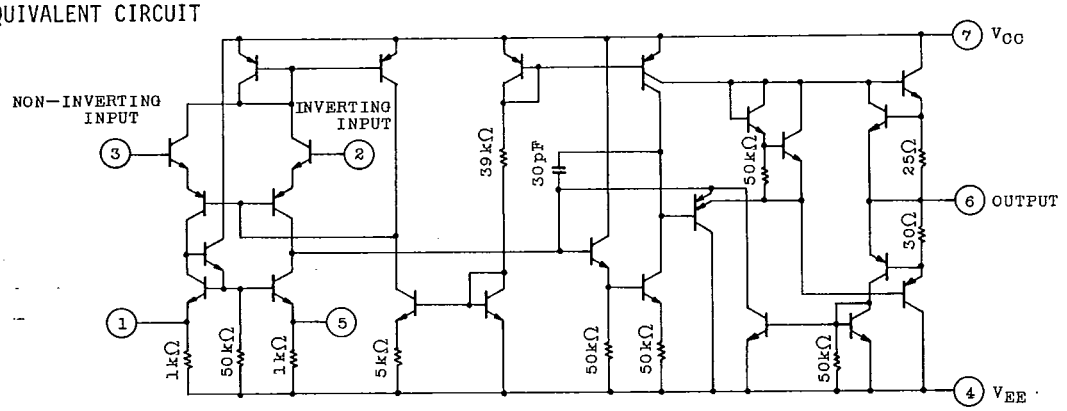
CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}, V_{EE}	±18	V
Differential Input Voltage		DV_{IN}	±30	V
Input Voltage		V_{IN}	V_{CC} ~ V_{EE}	V
Power Dissipation	TA7504P	P_D	300	mW
	TA7504S		400	
Operating Temperature		T_{opr}	-30 ~75	°C
Storage Temperature		T_{stg}	-55 ~125	°C

TA7504P/S

ELECTRICAL CHARACTERISTICS (V_{CC}=15V, V_{EE}=-15V, Ta=25°C)

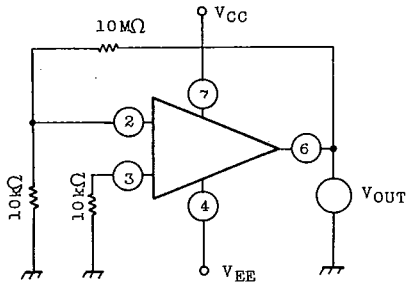
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Input Offset Voltage	V_{IO}	1	$R_g \leqq 10k\Omega$	-	1	5	mV
Input Offset Current	I_{IO}	2	-	-	30	200	nA
Input Bias Current	I_I	2	-	-	200	500	nA
Common Mode Input Voltage	CMV_{IN}	3	-	±12	±13	-	V
Maximum Output Voltage	V_{OM}	4	$R_L \geqq 10k\Omega$	±12	±14	-	V
	V_{OMR}		$R_L \geqq 2k\Omega$	±10	±13	-	
Maximum Output Voltage Swing	V_{Op-p}	5	R_L=10kΩ, f=1kHz	24	28	-	V
Output Short Circuit Current	I_{OS}	4	-	-	±20	-	mA
Input Impedance	Z_{IN}	-	f=1kHz	0.3	1	-	MΩ
Output Impedance	Z_{OUT}	-	f=1kHz	-	60	-	Ω
Voltage Gain	G_V	-	R_L=2kΩ, V_{OUT}=±10V f=10kHz	20	100	-	$\times 10^3$
Common Mode Input Signal Rejection Ratio	CMRR	3	CMV_{IN}=±10V, f=100Hz	70	90	-	dB
Supply Voltage Rejection Ratio	SVRR	1	$R_g \leqq 10k\Omega$	-	30	150	μV/V
Power Dissipation	P_D	6	-	-	50	85	mW
Temperature Coefficient of Input Offset Voltage	$\Delta V_{IO}/\Delta T$	1	$R_g \leqq 10k\Omega$, Ta=-30 ~ 75°C	-	5	50	μV/°C
Slew Rate	SR	7	R_L=2kΩ	-	0.5	-	V/μs
Rise Time	t_r	8	C_L=100pF, R_L=2kΩ	-	0.3	-	μs
Over Short	e_{over}			-	5	-	%
Input Noise Voltage	e_{np-p}	9	R_g=10kΩ, f=0 ~ 100Hz	-	6	-	μV

EQUIVALENT CIRCUIT



TEST CIRCUIT

(1) V_{IO}, $\Delta V_{IO}/\Delta T$, SVRR



$V_{IO}=V_{OUT}/1000$

$$SVRR = \frac{V_{OUT}-V_{OUT2}}{1000 \times 5}$$

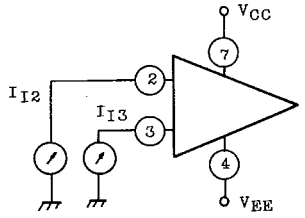
V_{OUT1} ; (V_{CC}, $-V_{EE}$ = 17.5(V)

V_{OUT2} ; (V_{CC}, $-V_{EE}$ = 12.5(V)

$\Delta V_{IO}/\Delta T=|V_{IO}(25^{\circ}C)-V_{IO}(-30^{\circ}C)|/55$

$\Delta V_{IO}/\Delta T=|V_{IO}(25^{\circ}C)-V_{IO}(75^{\circ}C)|/50$

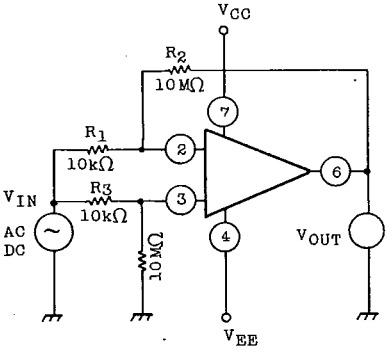
(2) I_I, I_{IO}



$I_{IO}=|I_{I2}-I_{I3}|$

$$I_I = \frac{I_{I2}+I_{I3}}{2}$$

(3) CMV_{IN}, CMRR

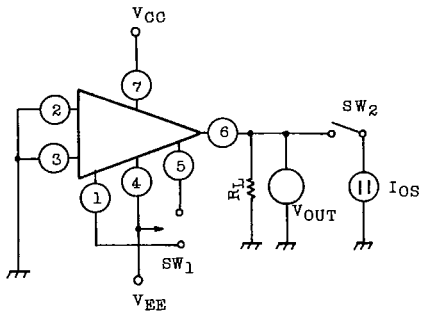


CMV_{IN} : $V_{OUT}=\pm 10(V_{DC})$, V_{IN} MEASURED

CMRR : $V_{IN}=7.07(V_{rms})$, V_{OUT} MEASURED

$$CMRR = 20 \log \frac{V_{IN}}{\frac{V_{OUT}}{1000}} = 20 \log \frac{7070}{V_{OUT}} \text{ (dB)}$$

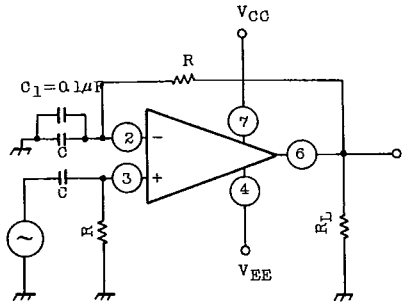
(4) V_{OM}, V_{OMR}, I_{OS}



V_{OM}, V_{OMR} : SW_2 : OPEN CIRCUIT
SW_1 : TERMINAL 1 OR 5

I_{OS} : SW_2 : SHORT CIRCUIT
SW_1 : TERMINAL 1 OR 5

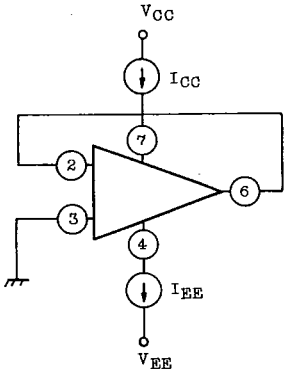
(5) G_V, V_{Op-p}



C : DC COUPLE

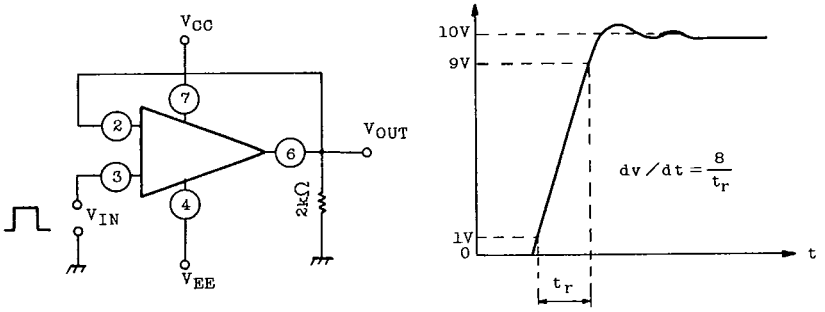
C_I : HF BYPASS
$\omega \gg 1/RC$
$G_V = V_{OUT}/V_{IN}$

(6) P_D

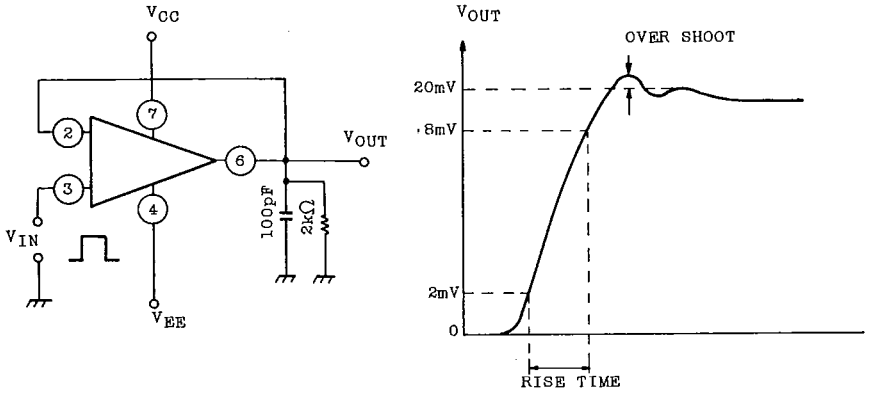


$P_D = (V_{CC}-V_{EE})\ I_{CC}$
$= (V_{CC}-V_{EE})\ I_{EE}$

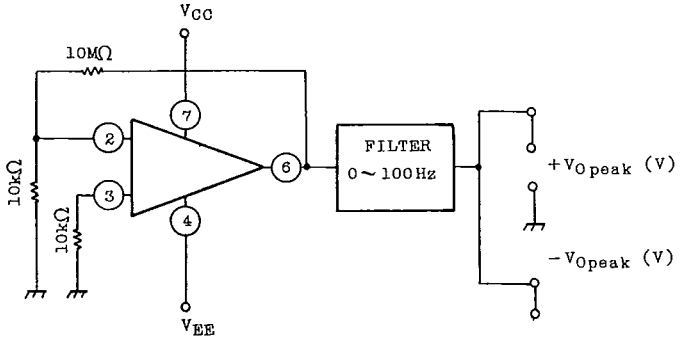
(7) SR



(8) RESPONSE TIME

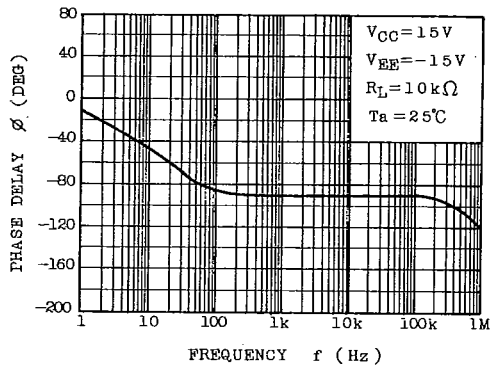


(9) e_{np-p}

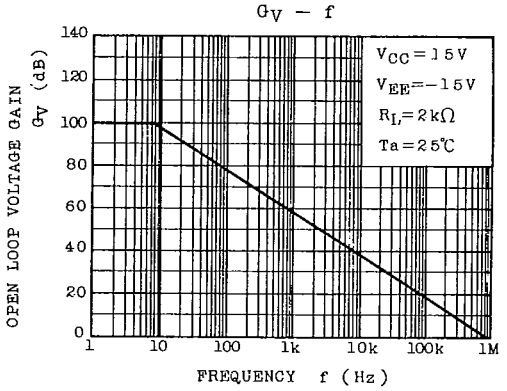


$e_{np-p} = (|+V_{Opeak}| + |-V_{Opeak}|) \times 10$ (V)

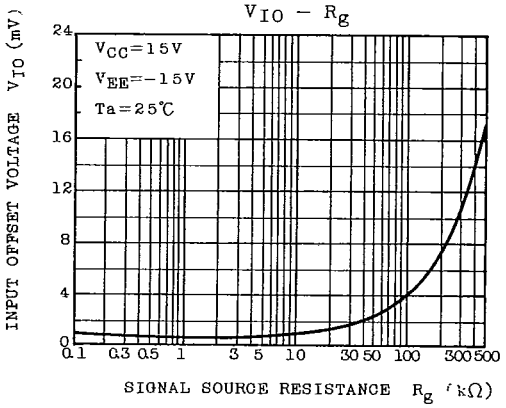
ϕ – f



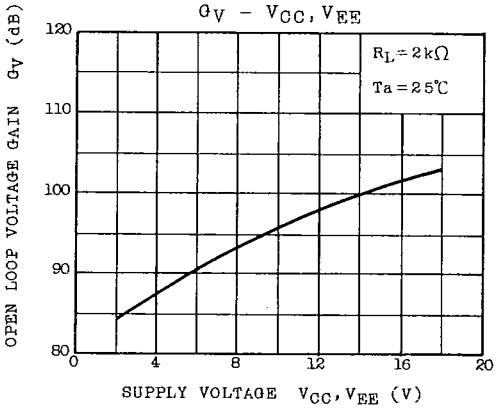
G_V – f



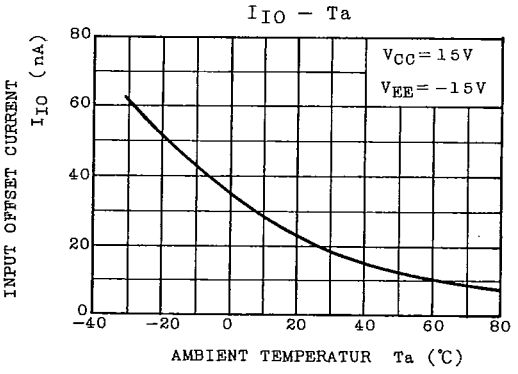
V_{IO} – R_g



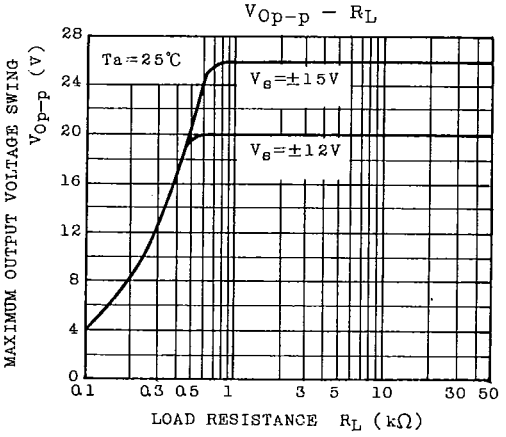
G_V – V_{CC}, V_{EE}



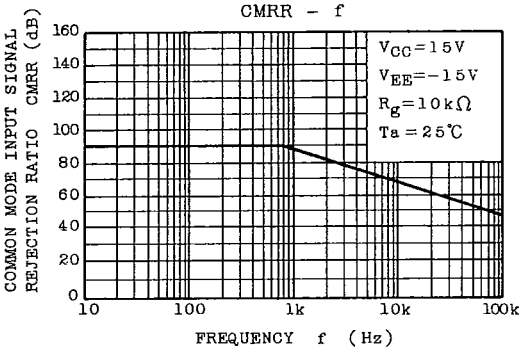
I_{IO} – Ta



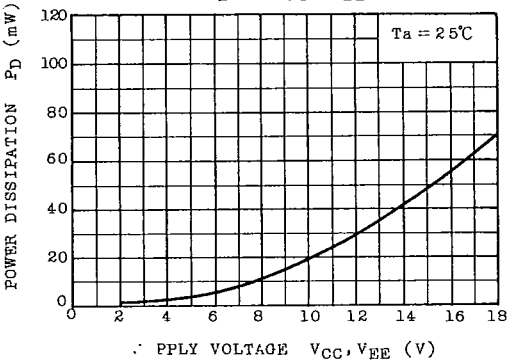
V_{Op-p} – R_L



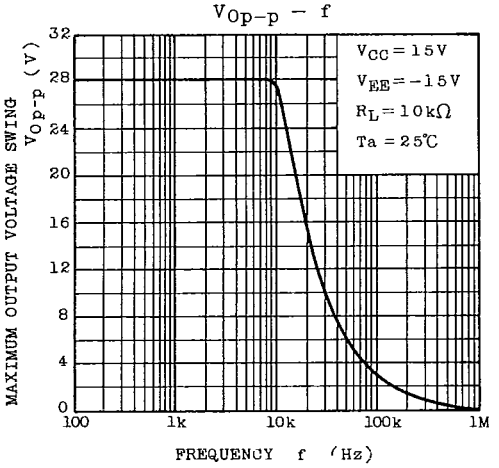
CMRR – f



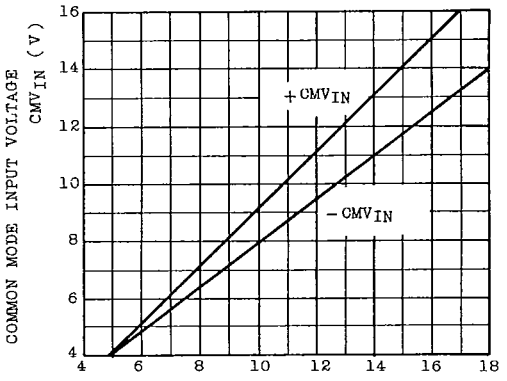
P_D – V_{CC}, V_{EE}



V_{Op-p} – f



CMV_{IN} – V_{CC}, V_{EE}



PULSE CHARACTERISTICS